Compal Confidential

HQD70/HDQ71 Schematics Document

Intel Dothan Processor with 915PM/915GM + DDRII + ICH6M

(With ATi M26-P)

2005-05-12

REV: 0.2 (For DVT)

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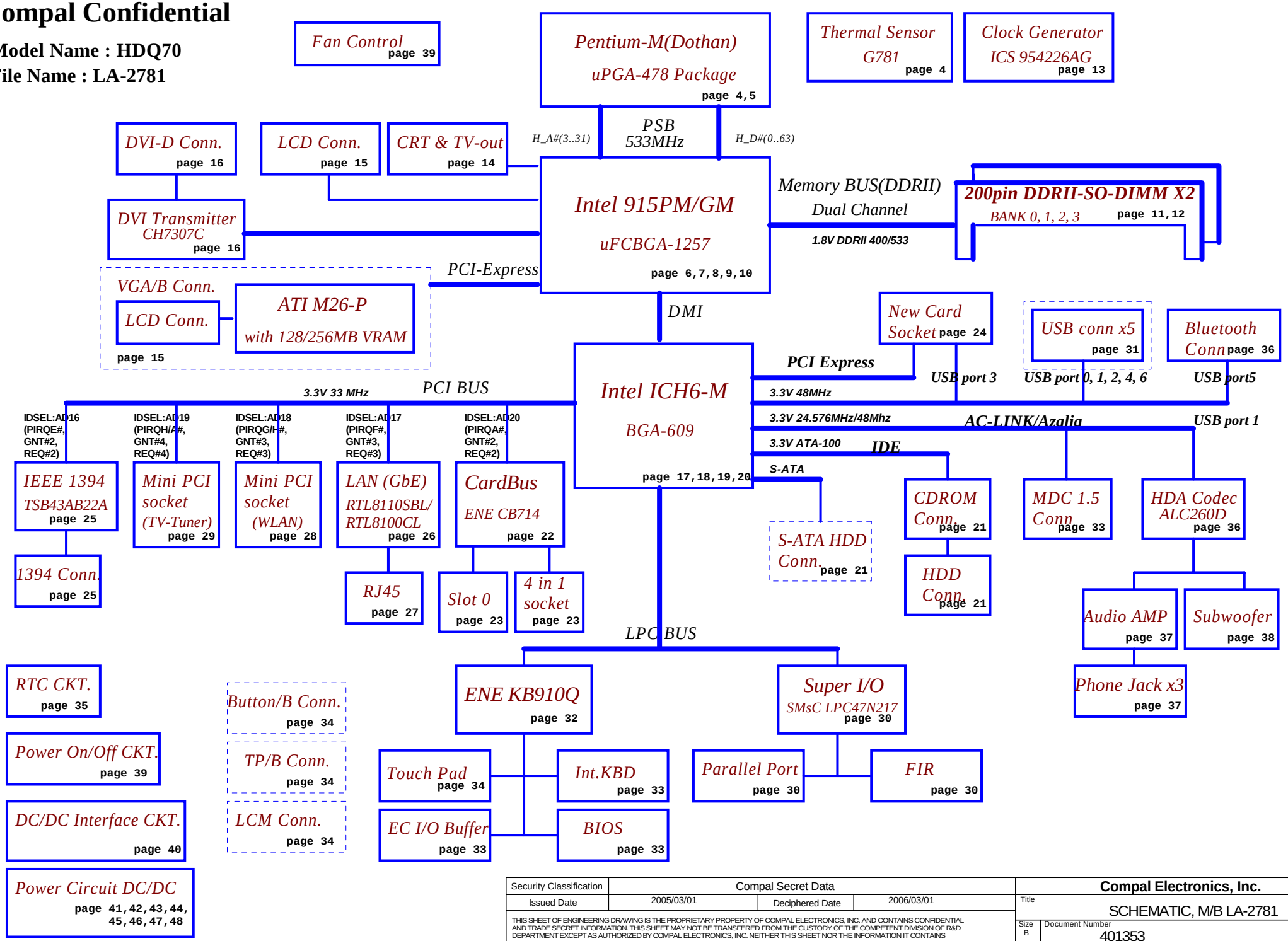
Model Name : HDQ70
File Name : LA-2781



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9VS	0.9V switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF
+1.5VALW	1.5V always on power rail	ON	ON	ON*
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
CardBus(SD)	AD20	2	PIRQA/PIRQB
1394	AD16	0	PIRQE
LAN	AD17	3	PIRQF
Mini-PCI(WLAN)	AD18	1	PIRQG/PORQH
Mini-PCI(TV-Tuer)	AD19	4	PIRQH/PORQA

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b
EEPROM(24C16/02)	1010 000X b
GMT G781-1	1001 110X b

EC SM Bus2 address

Device	Address
GMT G781	1001 110X b

ICH6M SM Bus address

Device	Address
Clock Generator (ICS 954226)	1101 001Xb
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%
Ra/Rc/Re	100K +/- 5%

Board ID	Rb / Rd / Rf	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

BTO Option Table

BTO Item	BOM Structure
VGA	@PM @GM
LAN	@8110S @8100C
LCM	@LCM @NO_LCM

SKU ID Table

SKU ID	SKU
0	PM
1	GM
2	
3	
4	
5	
6	
7	

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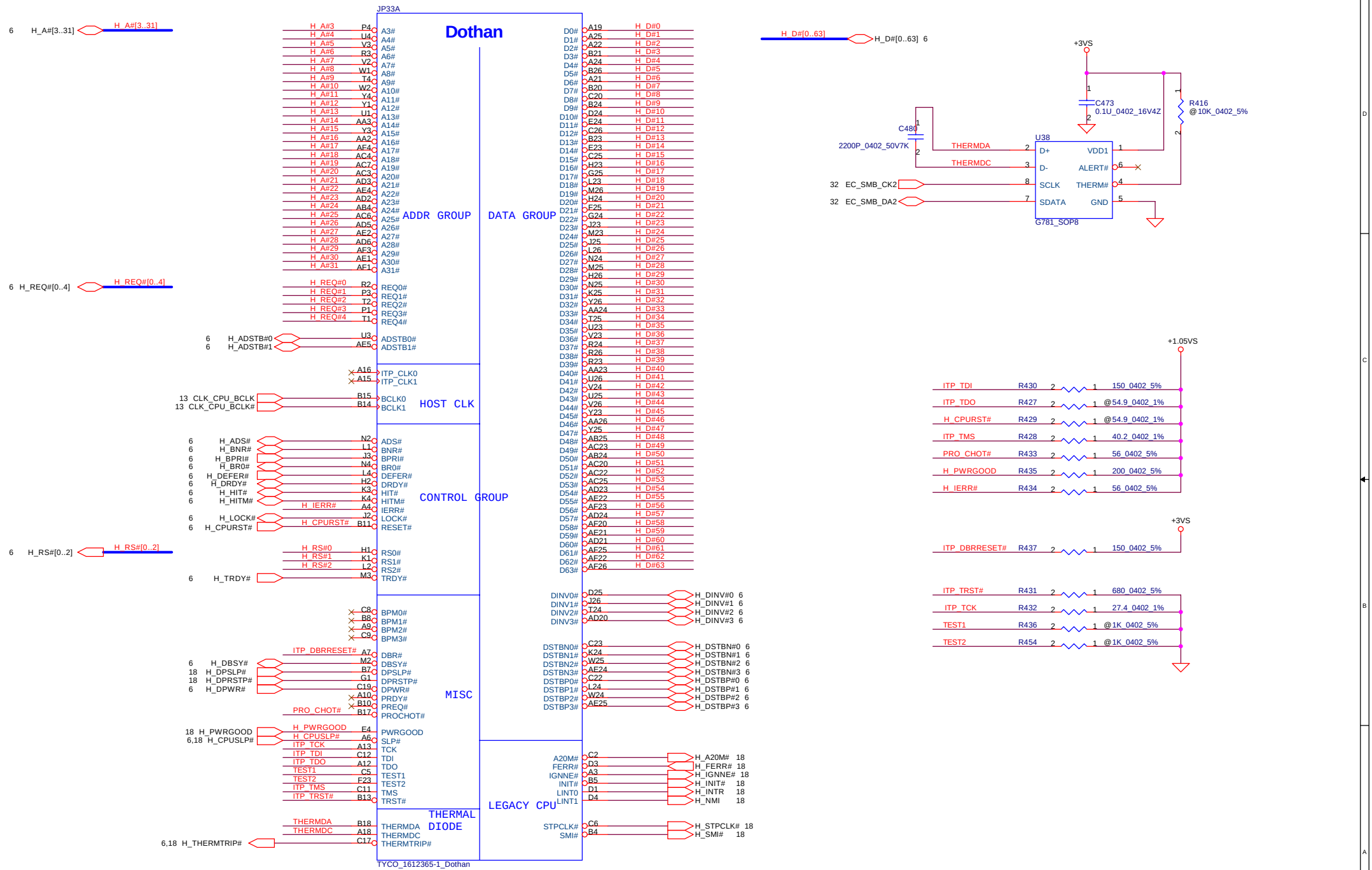

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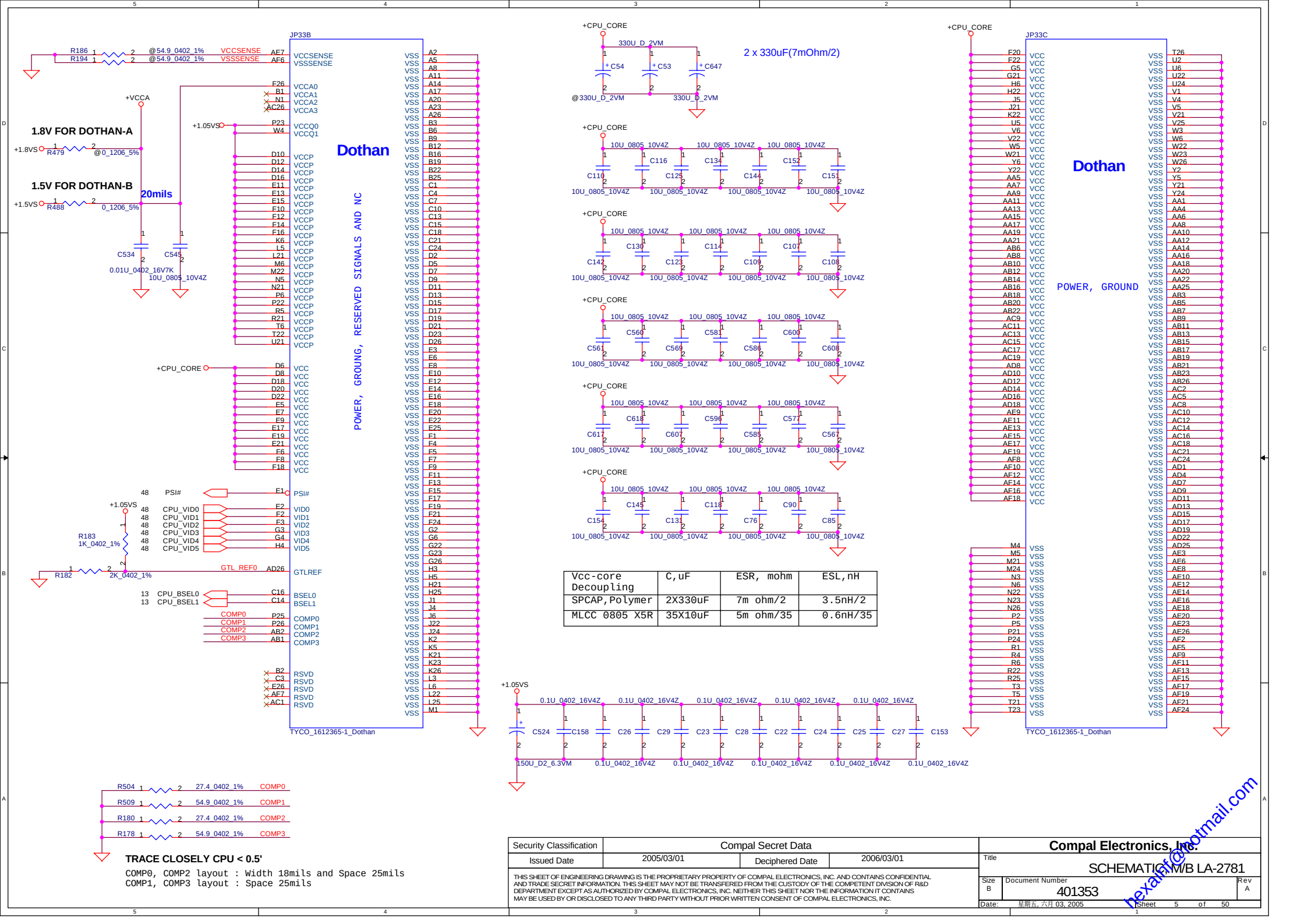

Vcc-core Decoupling	C,uF	ESR, mohm	ESL,nH
SPCAP,Polymer	2X330uF	7m ohm/2	3.5nH/2
MLCC 0805 X5R	35X10uF	5m ohm/35	0.6nH/35

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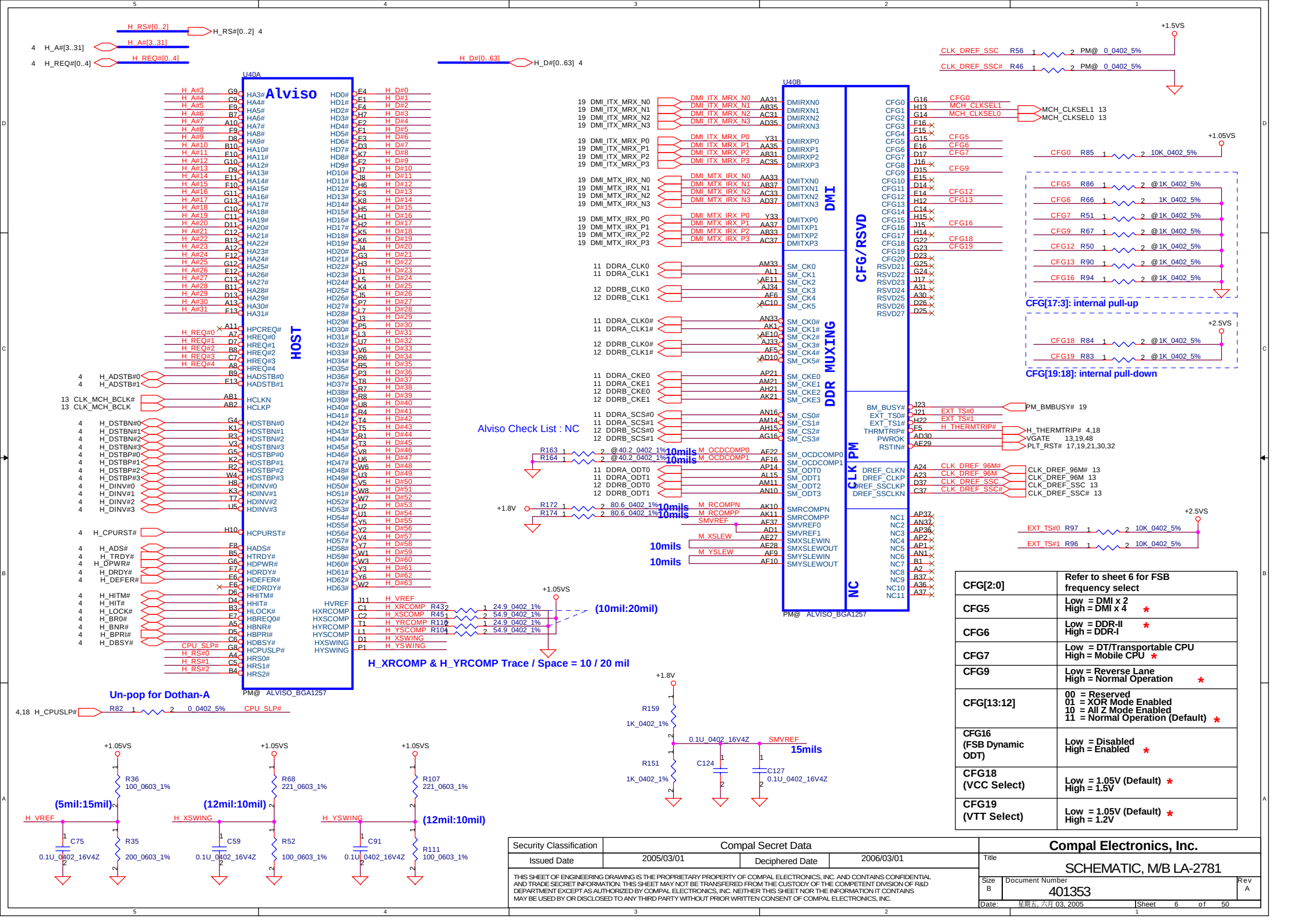

CFG[2:0]	Refer to sheet 6 for FSB frequency select
CFG5	Low = DMI x 2 High = DMI x 4 *
CFG6	Low = DDR-II * High = DDR-I
CFG7	Low = DT/Transportable CPU High = Mobile CPU *
CFG9	Low = Reverse Lane High = Normal Operation *
CFG[13:12]	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation (Default) *
CFG16 (FSB Dynamic ODT)	Low = Disabled High = Enabled *
CFG18 (VCC Select)	Low = 1.05V (Default) * High = 1.5V
CFG19 (VTT Select)	Low = 1.05V (Default) * High = 1.2V

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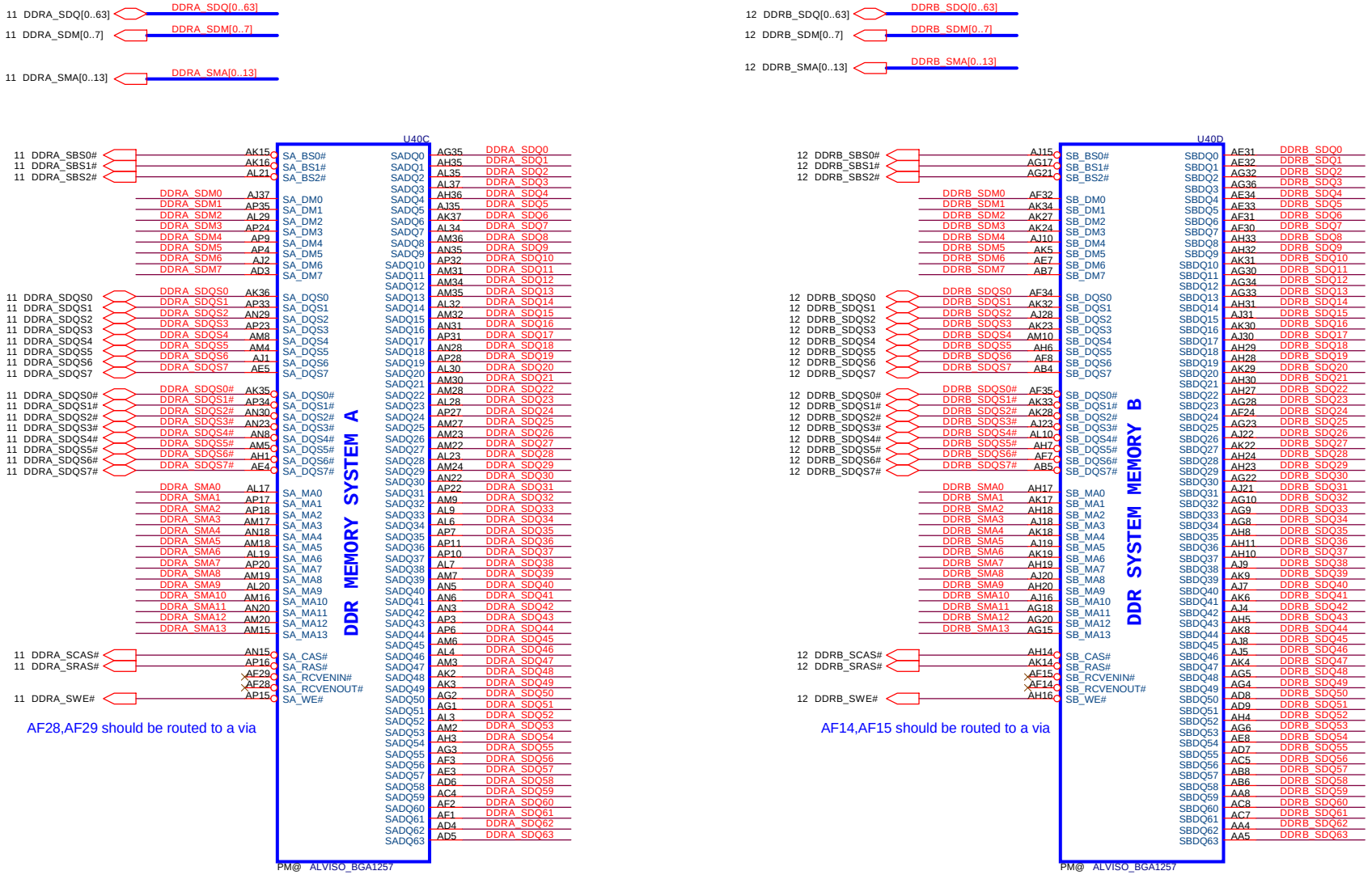

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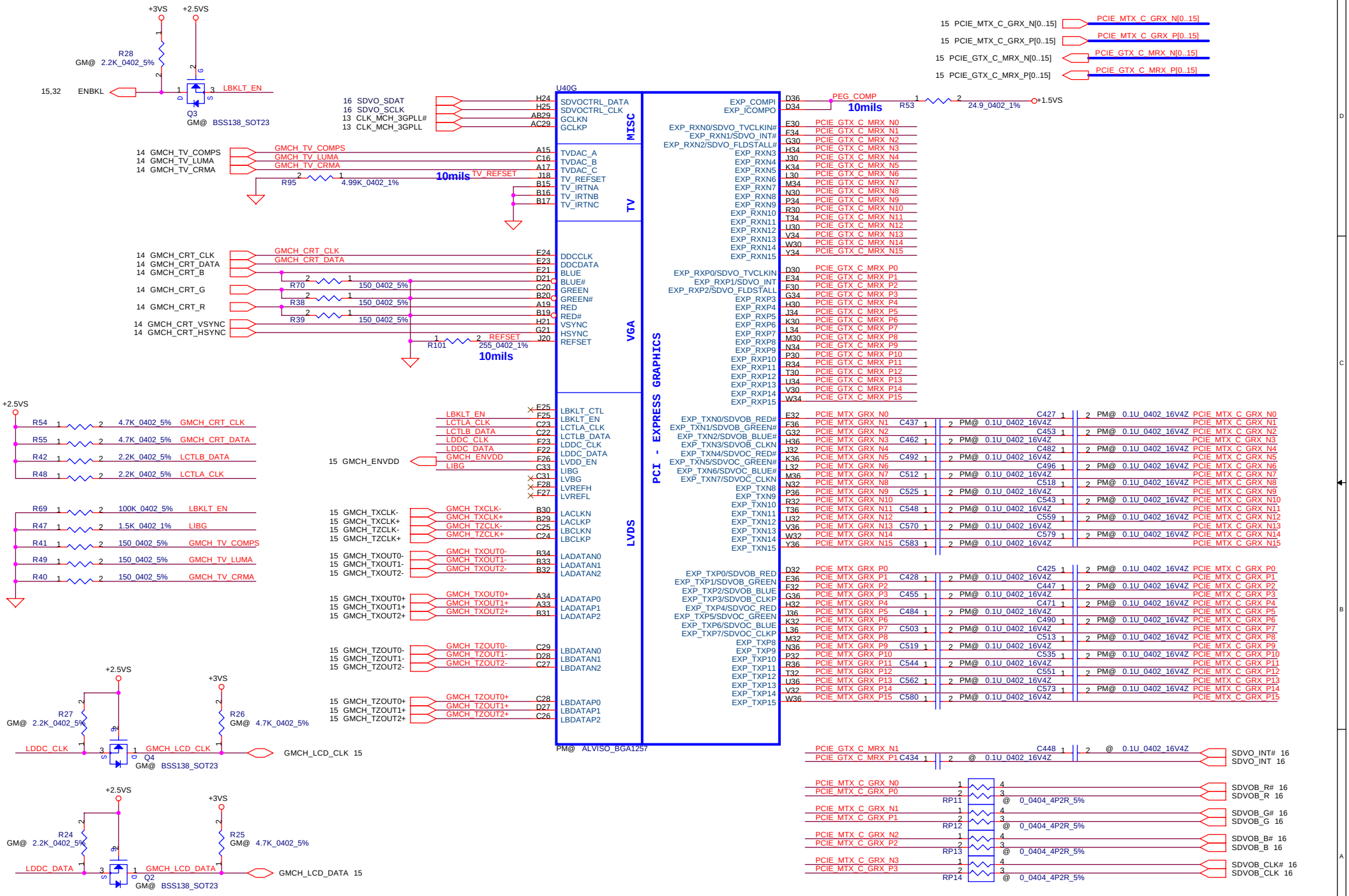

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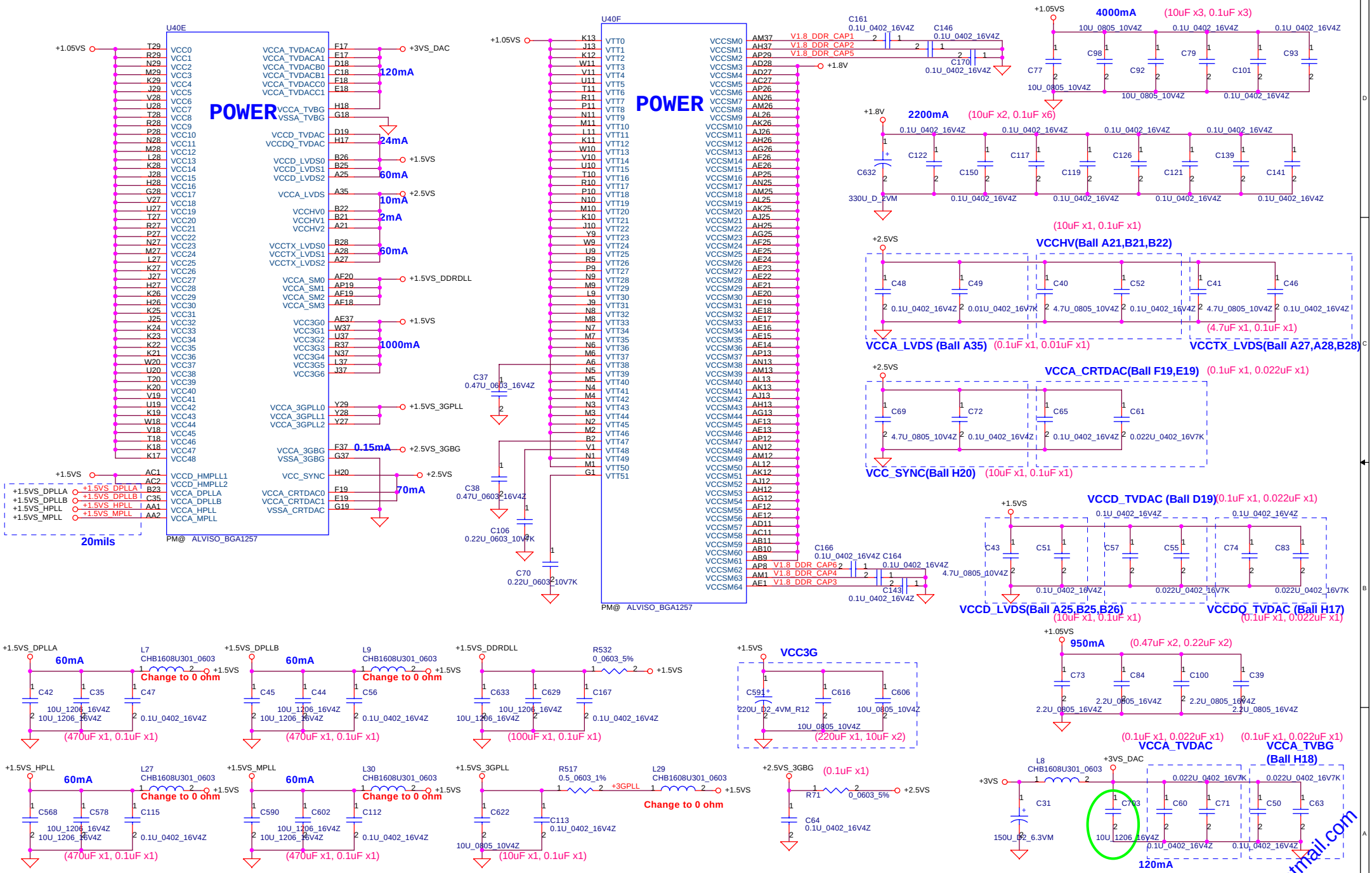

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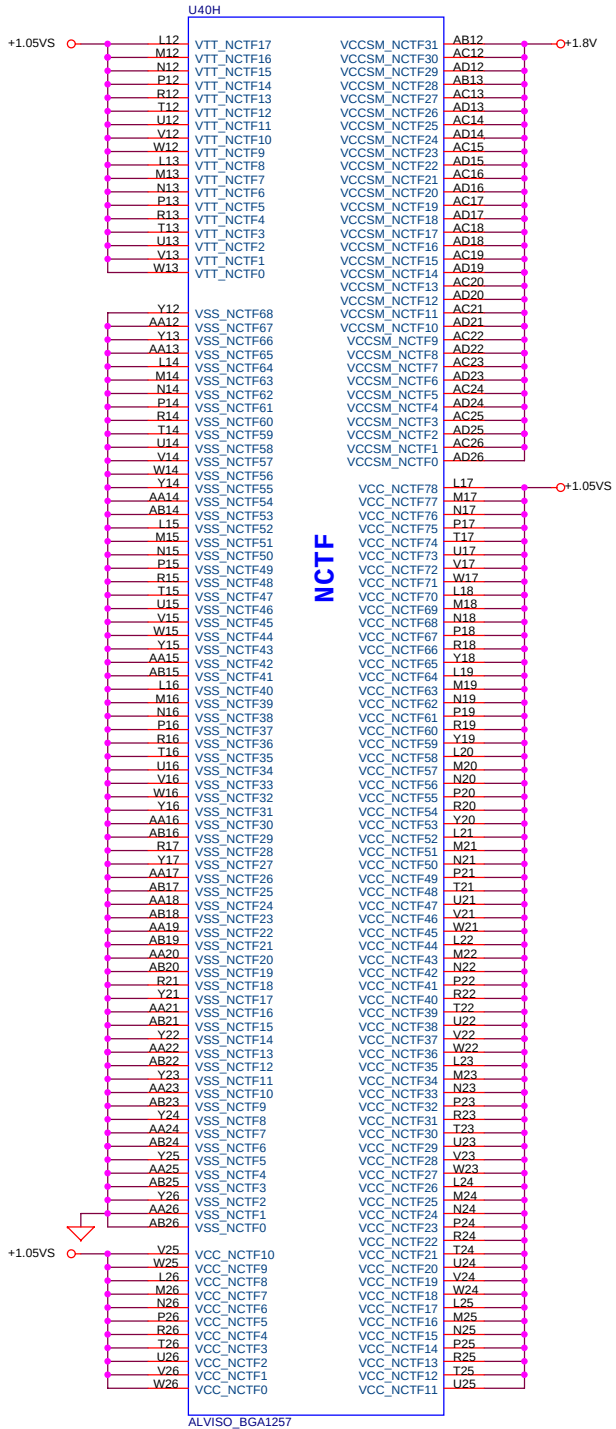

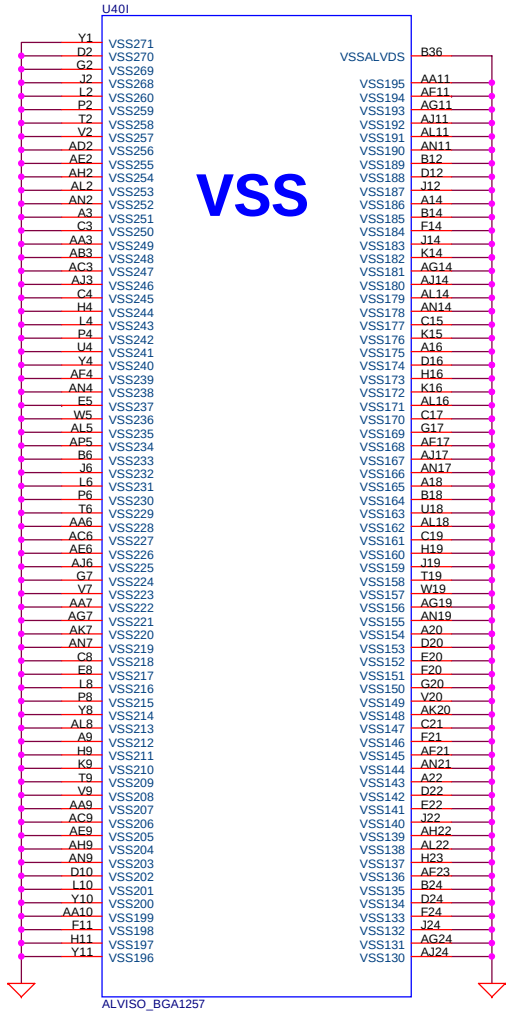

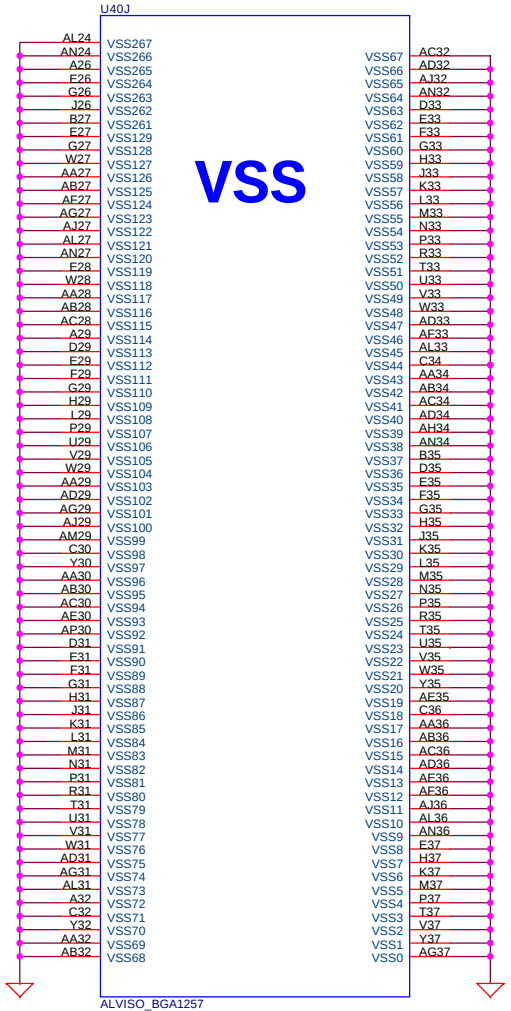

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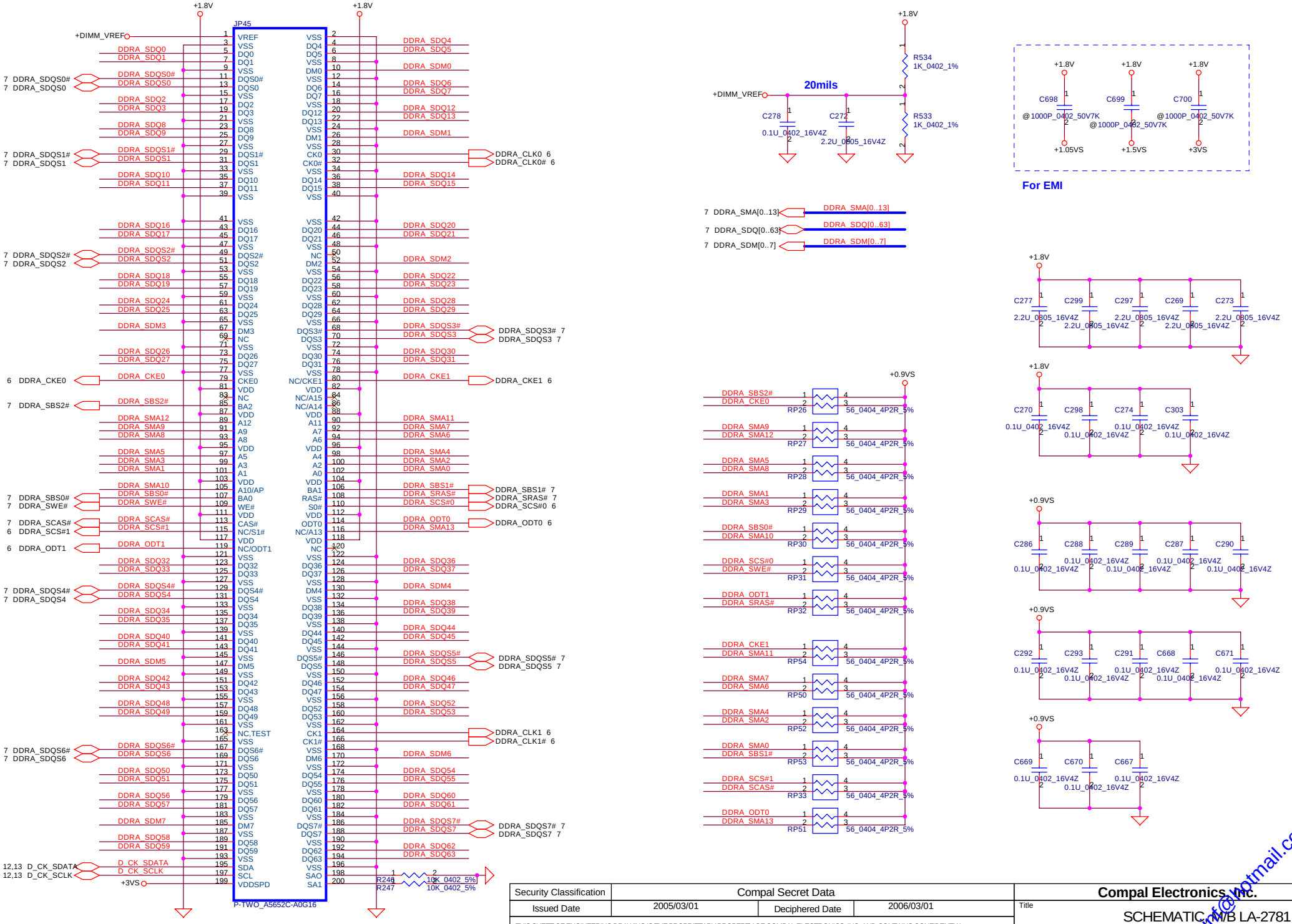

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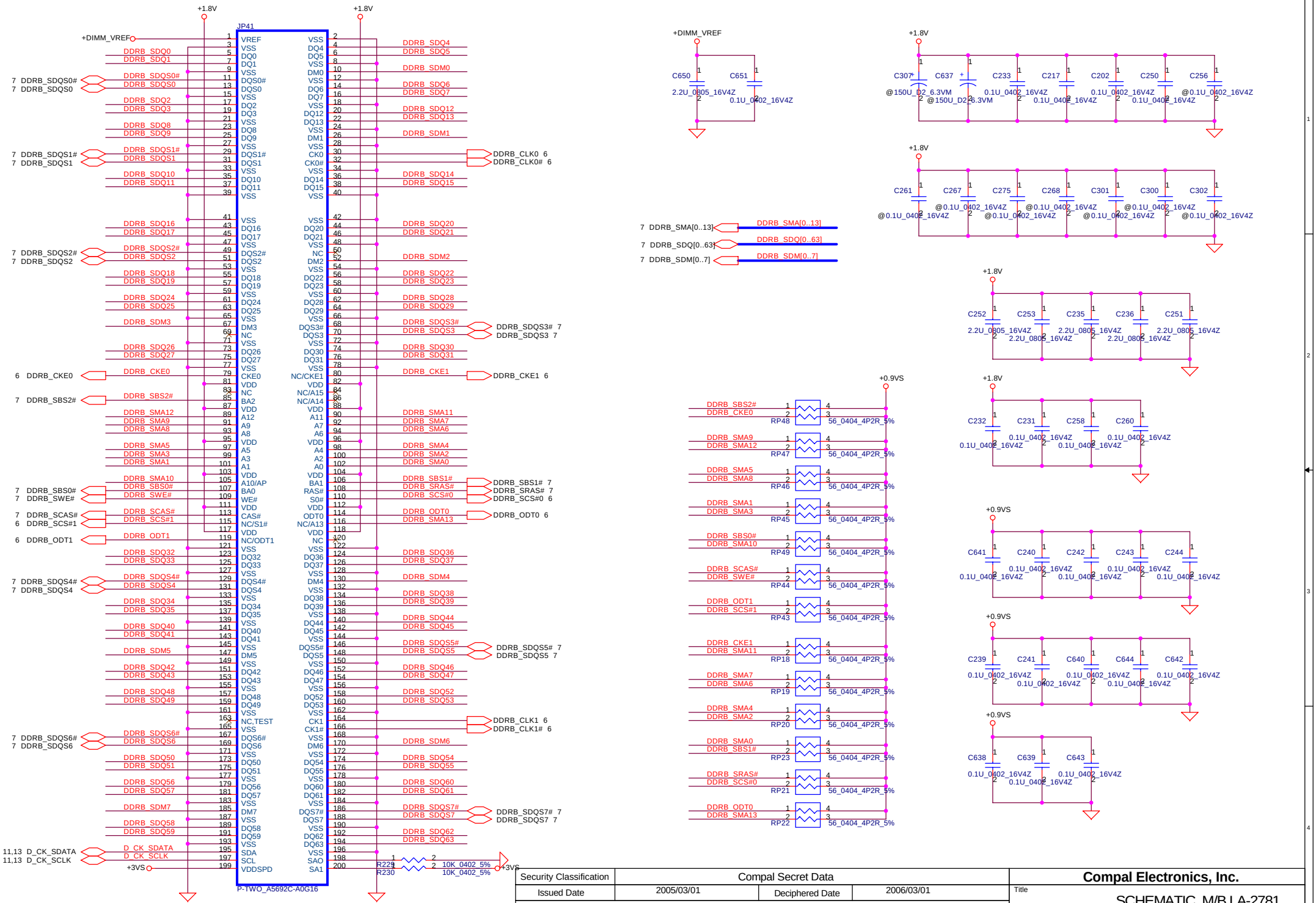

DIMM1 STD H:9.2mm (BOT)

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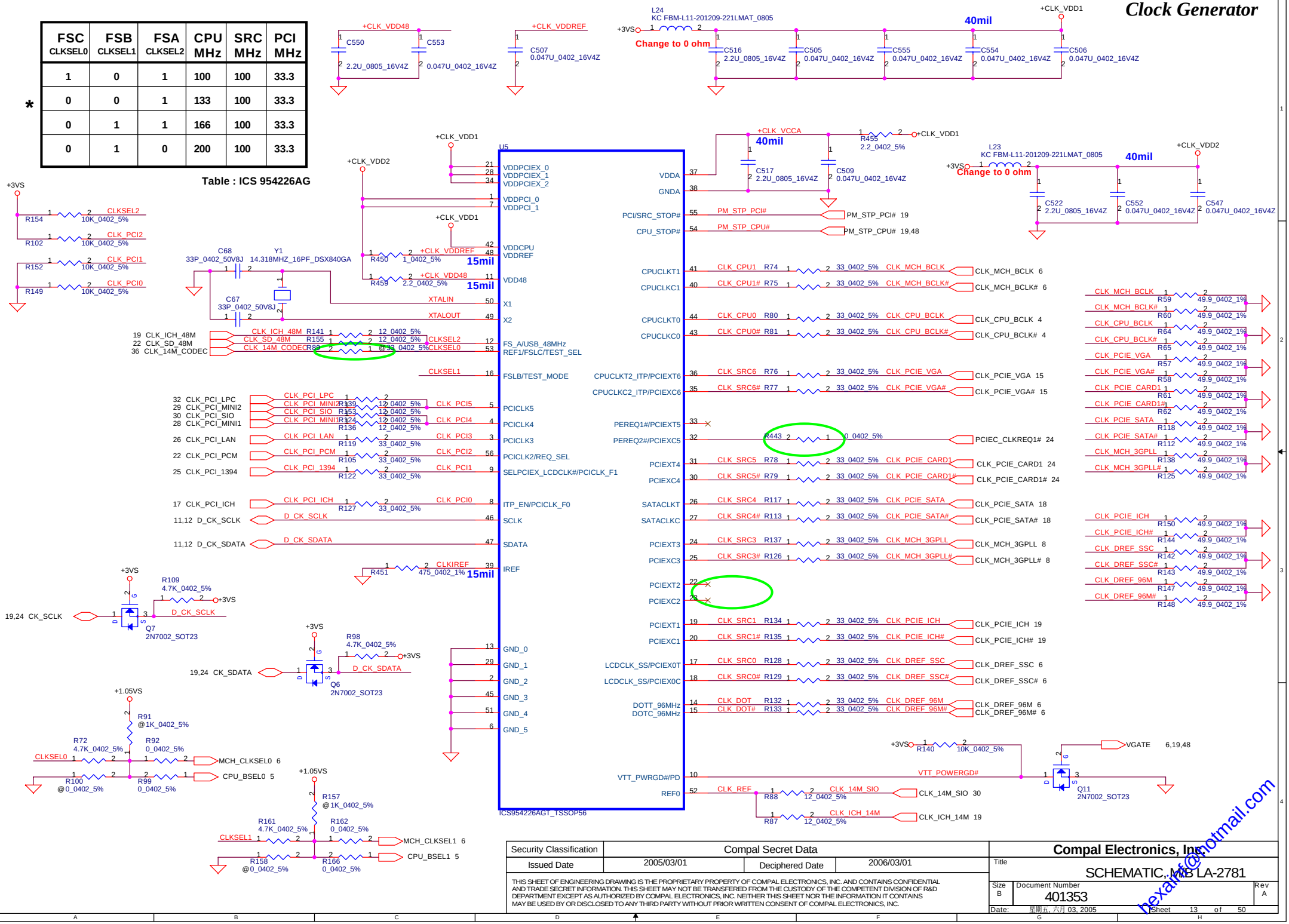
Clock Generator

	FSC CLKSEL0	FSB CLKSEL1	FSA CLKSEL2	CPU MHz	SRC MHz	PCI MHz
*	1	0	1	100	100	33.3
	0	0	1	133	100	33.3
	0	1	1	166	100	33.3
	0	1	0	200	100	33.3

Table : ICS 954226AG



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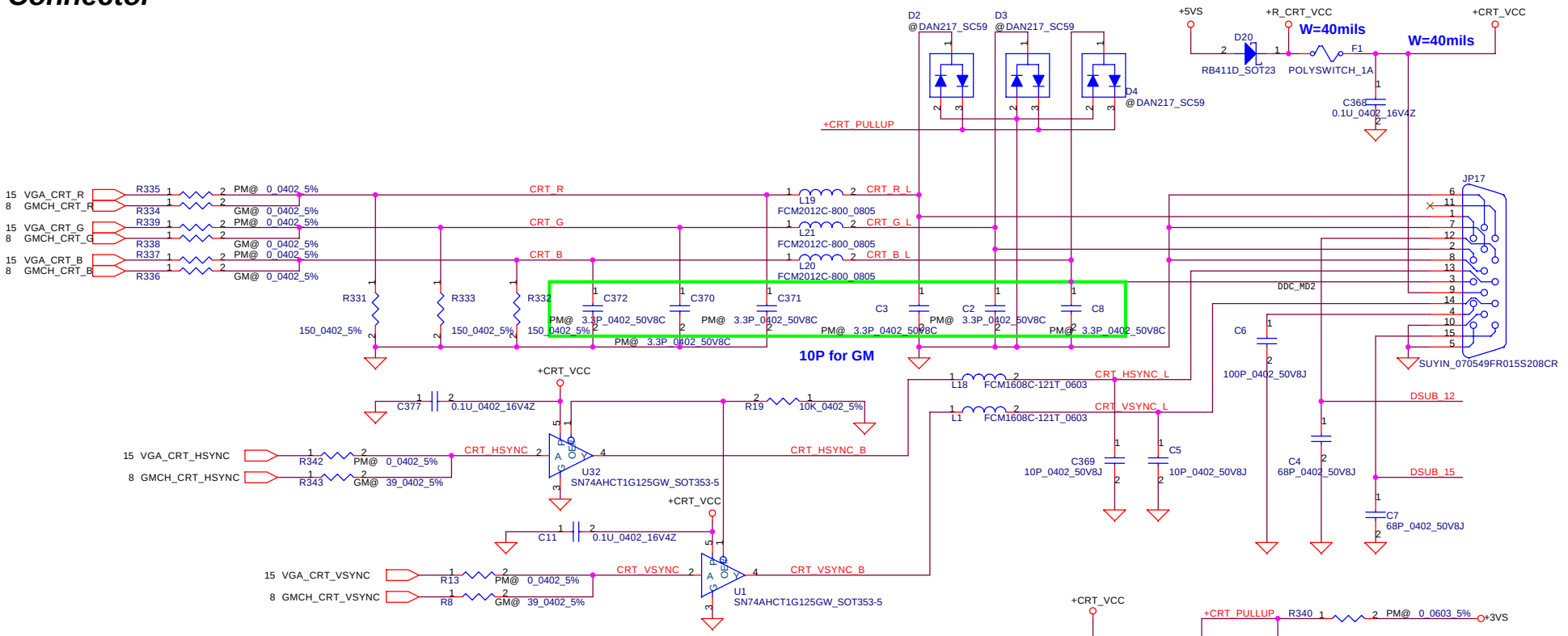
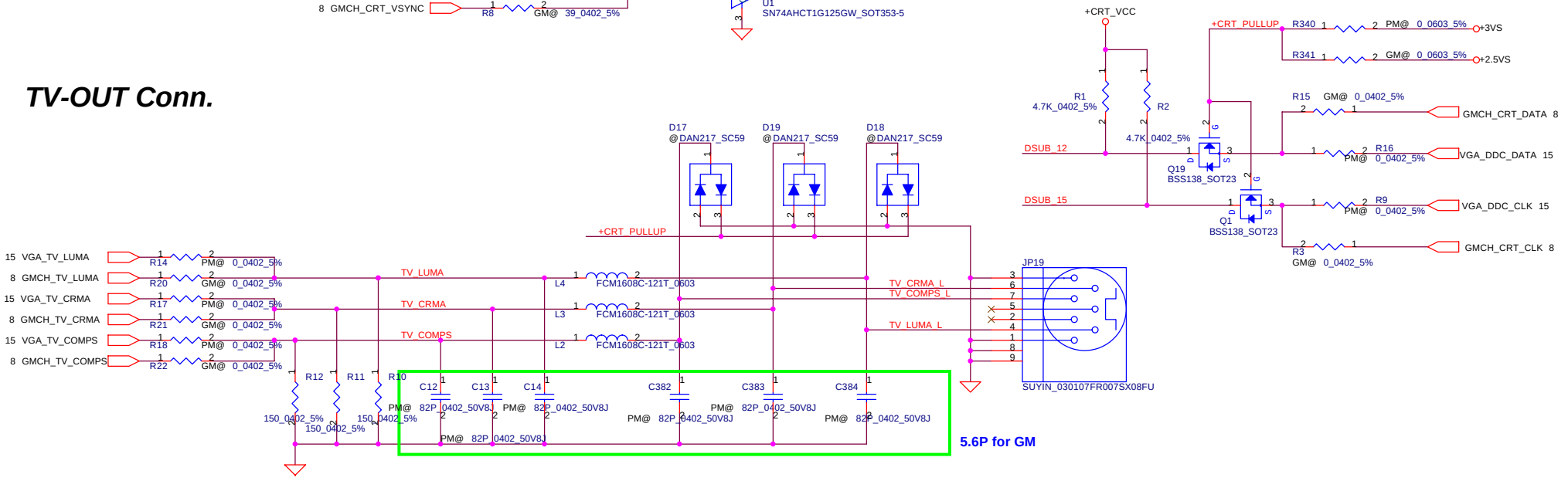
CRT Connector



TV-OUT Conn.



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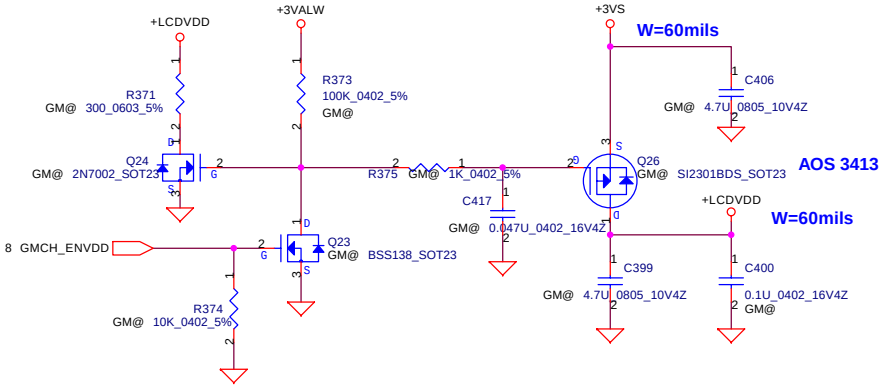
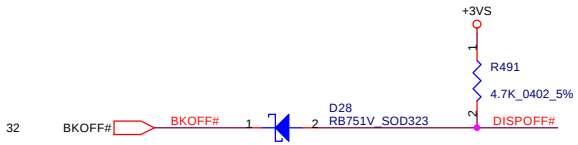
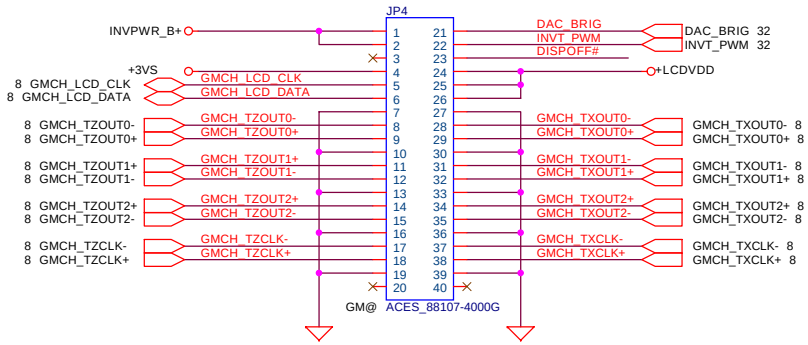
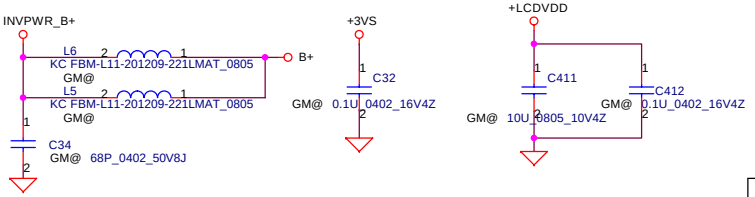
LCD POWER CIRCUIT

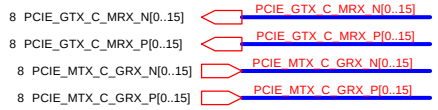




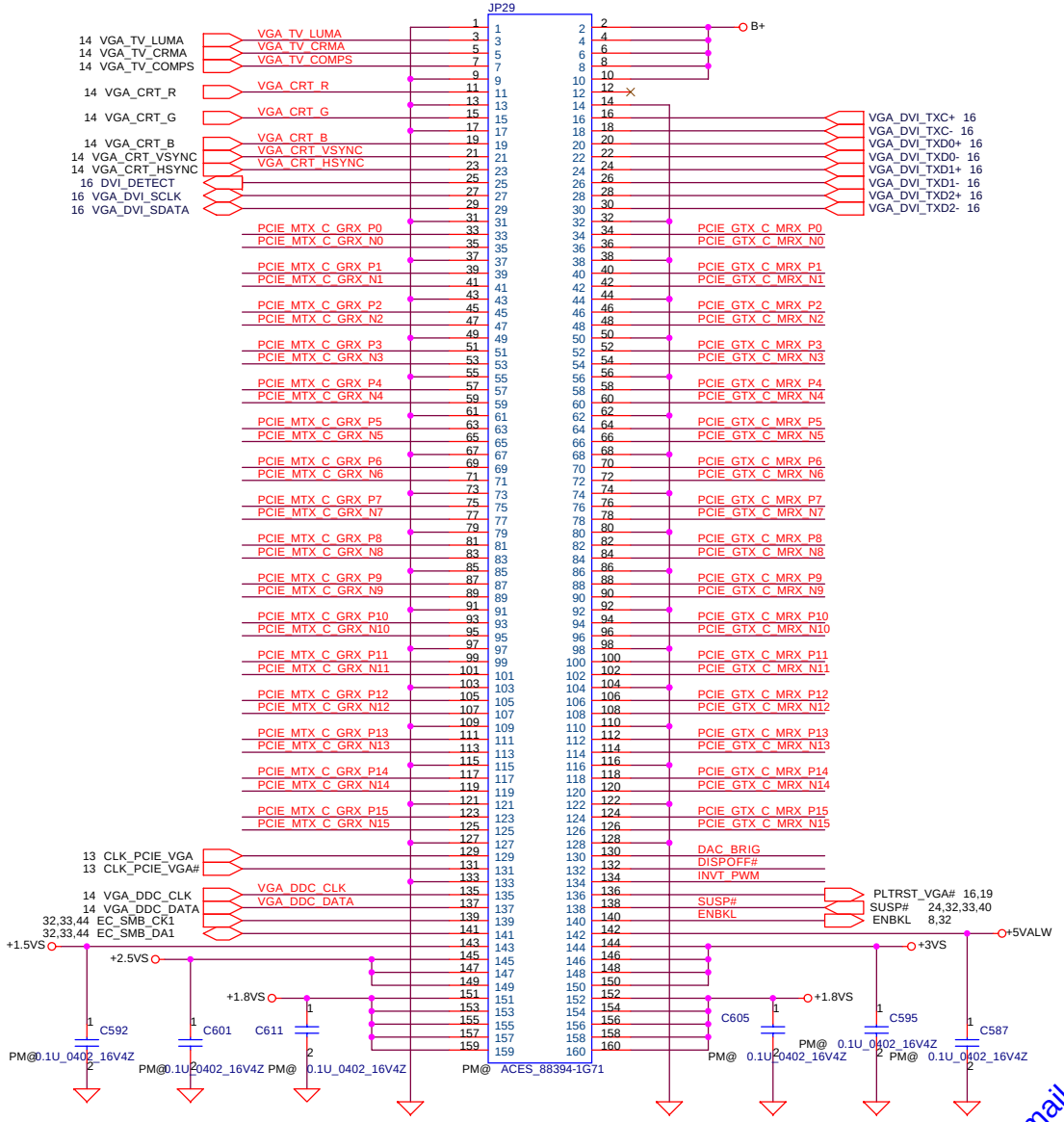
LCD Conn.







VGA BOARD Conn.



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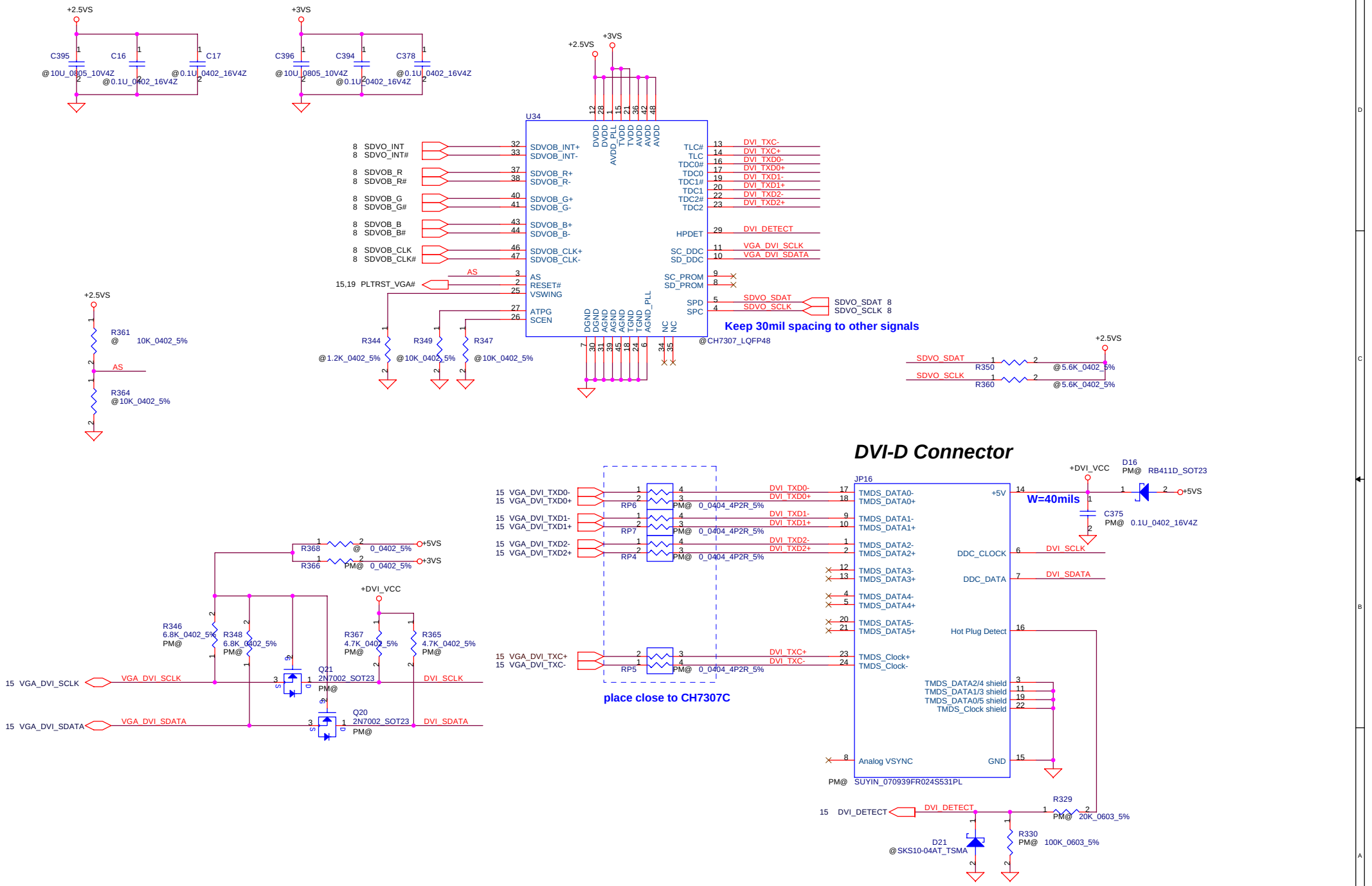

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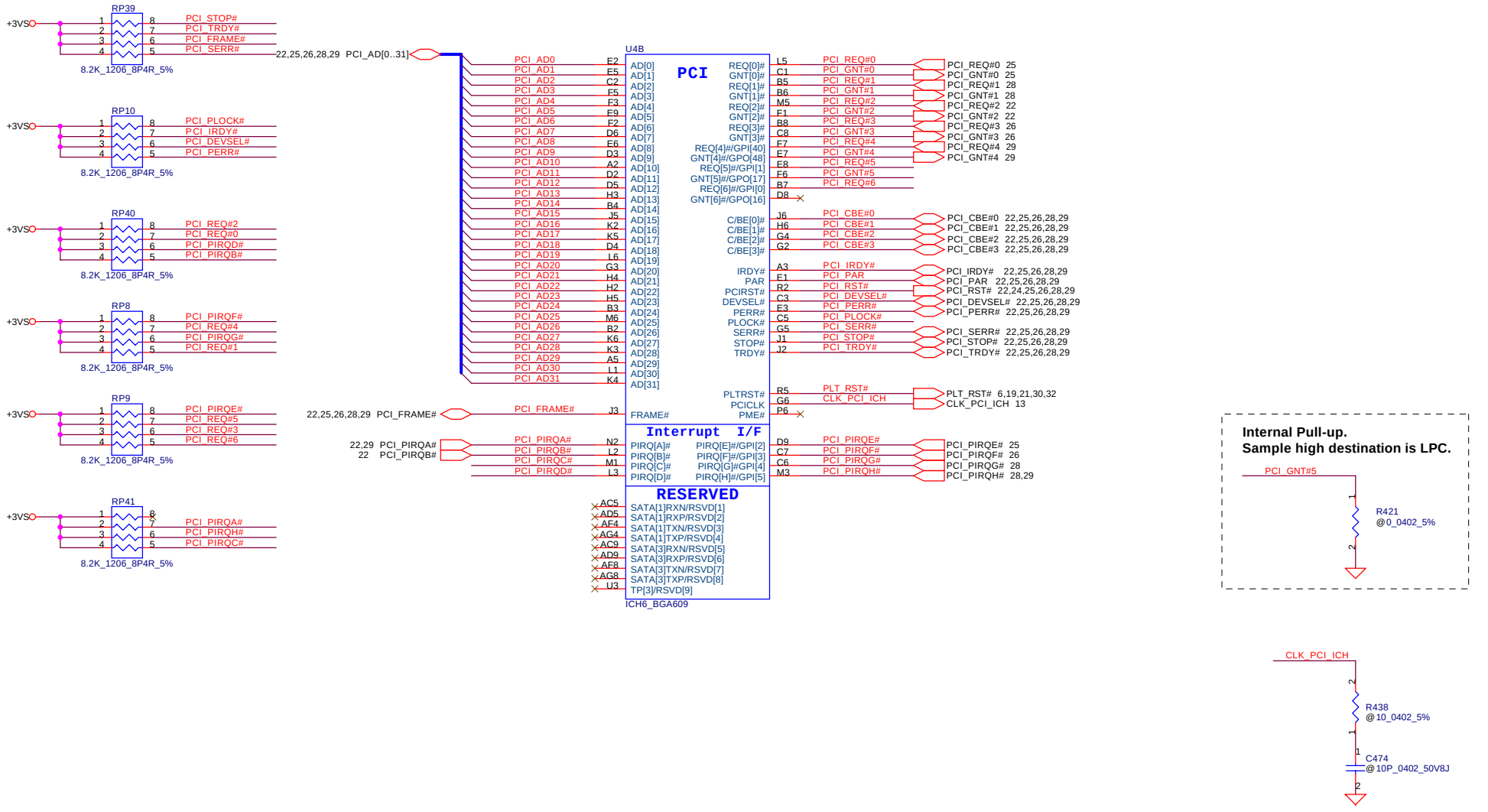

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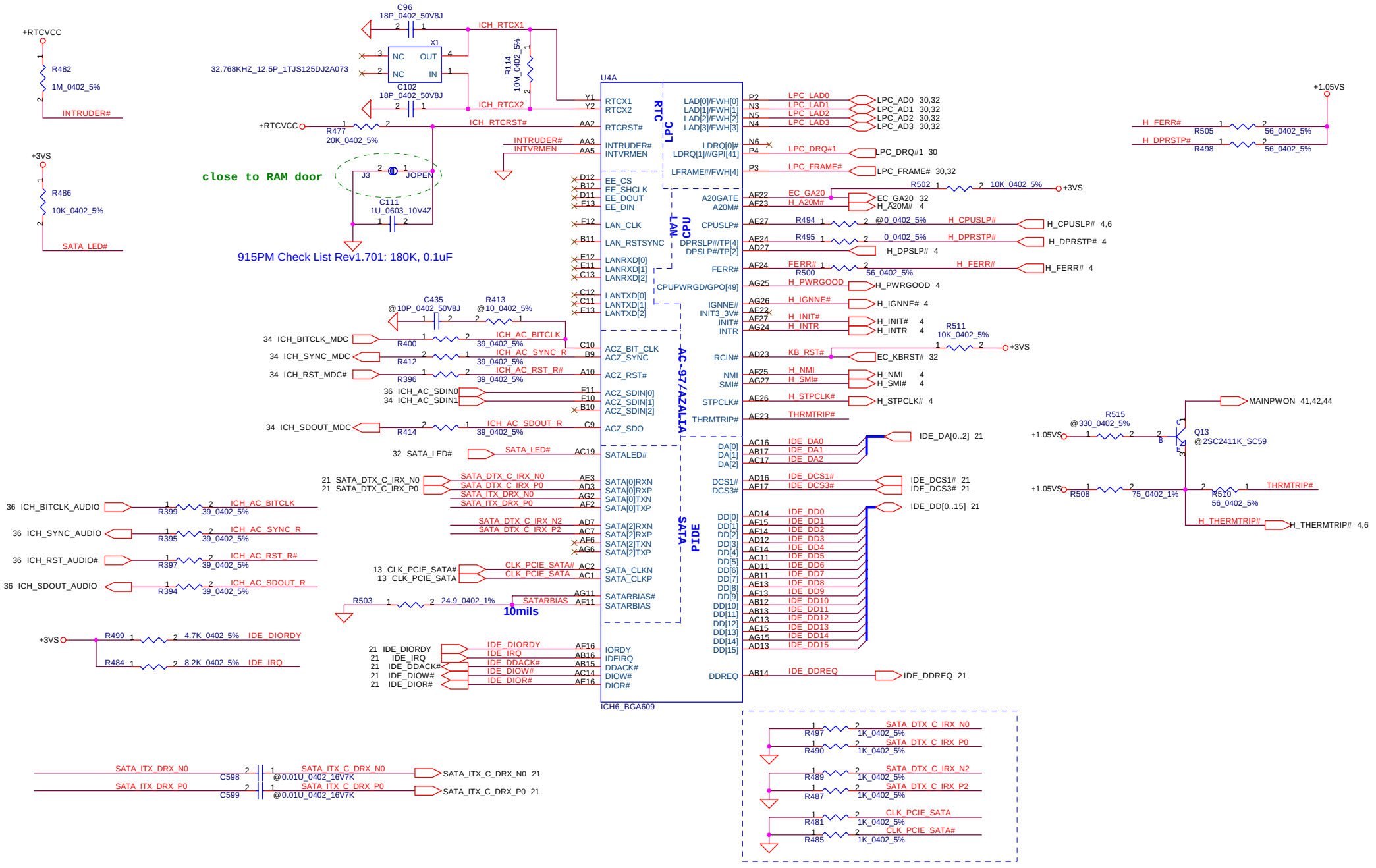

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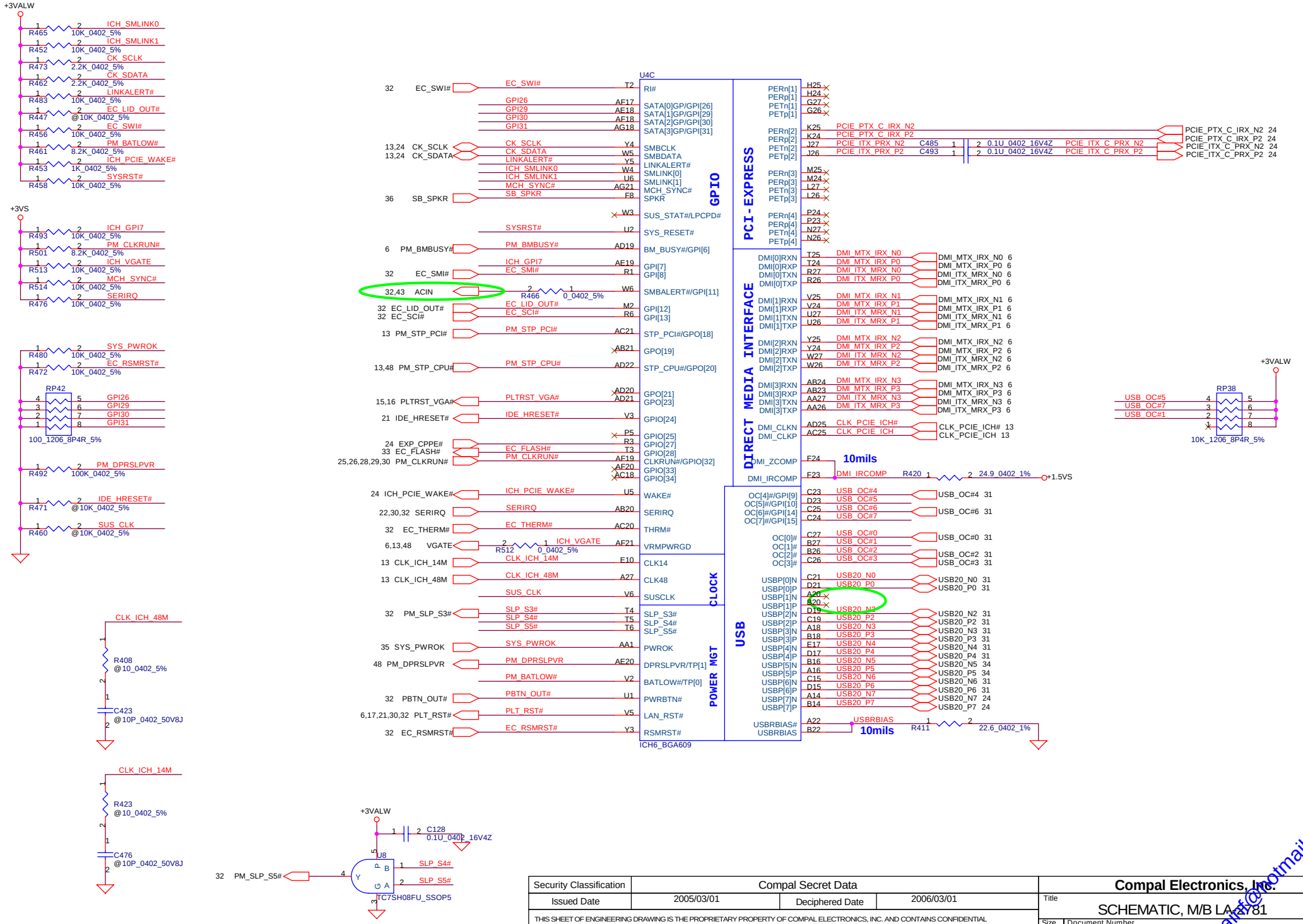
+3VALW
R465 10K_0402_5%
ICH_SMLINK0
R452 10K_0402_5%
ICH_SMLINK1
R473 2.2K_0402_5%
CK_SCLK
R462 2.2K_0402_5%
CK_SDATA
R483 10K_0402_5%
LINKALERT#
R447 @10K_0402_5%
EC_LID_OUT#
R456 10K_0402_5%
EC_SWI#
R461 8.2K_0402_5%
PM_BATLOW#
R453 1K_0402_5%
ICH_PCIE_WAKE#
R458 10K_0402_5%
SYSRST#
+3VS
R493 10K_0402_5%
ICH_GPI7
R501 8.2K_0402_5%
PM_CLKRUN#
R513 10K_0402_5%
ICH_VGATE
R514 10K_0402_5%
MCH_SYNC#
R476 10K_0402_5%
SERIRQ
R480 10K_0402_5%
SYS_PWROK
R472 10K_0402_5%
EC_RSMRST#
RP42
100_1206_8P4R_5%
GPI26
GPI29
GPI30
GPI31
R492 100K_0402_5%
PM_DPRSLPVR
R471 @10K_0402_5%
IDE_HRESET#
R460 @10K_0402_5%
SUS_CLK
CLK_ICH_48M
R408 @10_0402_5%
C423 @10P_0402_50V8J
CLK_ICH_14M
R423 @10_0402_5%
C476 @10P_0402_50V8J
U4C
ICH6_BGA609
GPIO
CLOCK
POWER MGT
PCI-EXPRESS
DIRECT MEDIA INTERFACE
USB
EC_SWI#
CK_SCLK
CK_SDATA
LINKALERT#
ICH_SMLINK0
ICH_SMLINK1
MCH_SYNC#
SB_SPKR
SUS_STAT#/LPCPD#
SYS_RESET#
PM_BMBUSY#
ICH_GPI7
EC_SMI#
ACIN
R466 0_0402_5%
SMBALERT#/GPI[11]
EC_LID_OUT#
EC_SCI#
PM_STP_PCI#
PM_STP_CPU#
PLTRST_VGA#
IDE_HRESET#
EXP_CPPE#
EC_FLASH#
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SERIRQ
EC_THERM#
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CLK_ICH_48M
SUS_CLK
SLP_S3#
SLP_S4#
SLP_S5#
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PM_BATLOW#
PBTN_OUT#
PLT_RST#
EC_RSMRST#
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PERp[1]
PETn[1]
PETp[1]
PERn[2]
PERp[2]
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DMI[3]RXN
DMI[3]RXP
DMI[3]TXN
DMI[3]TXP
DMI_CLKN
DMI_CLKP
DMI_ZCOMP
DMI_IRCOMP
R420 24.9_0402_1%
+1.5VS
10mils
OC[4]#/GPI[9]
OC[5]#/GPI[10]
OC[6]#/GPI[14]
OC[7]#/GPI[15]
OC[0]#
OC[1]#
OC[2]#
OC[3]#
USBP[0]N
USBP[0]P
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RP38
USB_OC#5
USB_OC#7
USB_OC#1
10K_1206_8P4R_5%
C128 0.1U_0402_16V4Z
U8
TC7SH08FU_SSOP5
32 EC_SWI#
13,24 CK_SCLK
13,24 CK_SDATA
36 SB_SPKR
6 PM_BMBUSY#
32 EC_SMI#
32,43 ACIN
32 EC_LID_OUT#
32 EC_SCI#
13 PM_STP_PCI#
13,48 PM_STP_CPU#
15,16 PLTRST_VGA#
21 IDE_HRESET#
24 EXP_CPPE#
33 EC_FLASH#
25,26,28,29,30 PM_CLKRUN#
24 ICH_PCIE_WAKE#
22,30,32 SERIRQ
32 EC_THERM#
6,13,48 VGATE
13 CLK_ICH_14M
13 CLK_ICH_48M
32 PM_SLP_S3#
35 SYS_PWROK
48 PM_DPRSLPVR
32 PBTN_OUT#
6,17,21,30,32 PLT_RST#
32 EC_RSMRST#
32 PM_SLP_S5#
Security Classification
Compal Secret Data
Issued Date
2005/03/01
Deciphered Date
2006/03/01
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Compal Electronics, Inc.
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SCHEMATIC, M/B LA-2781
Size B
Document Number
401353
Rev A
Date: 星期五, 六月 03, 2005
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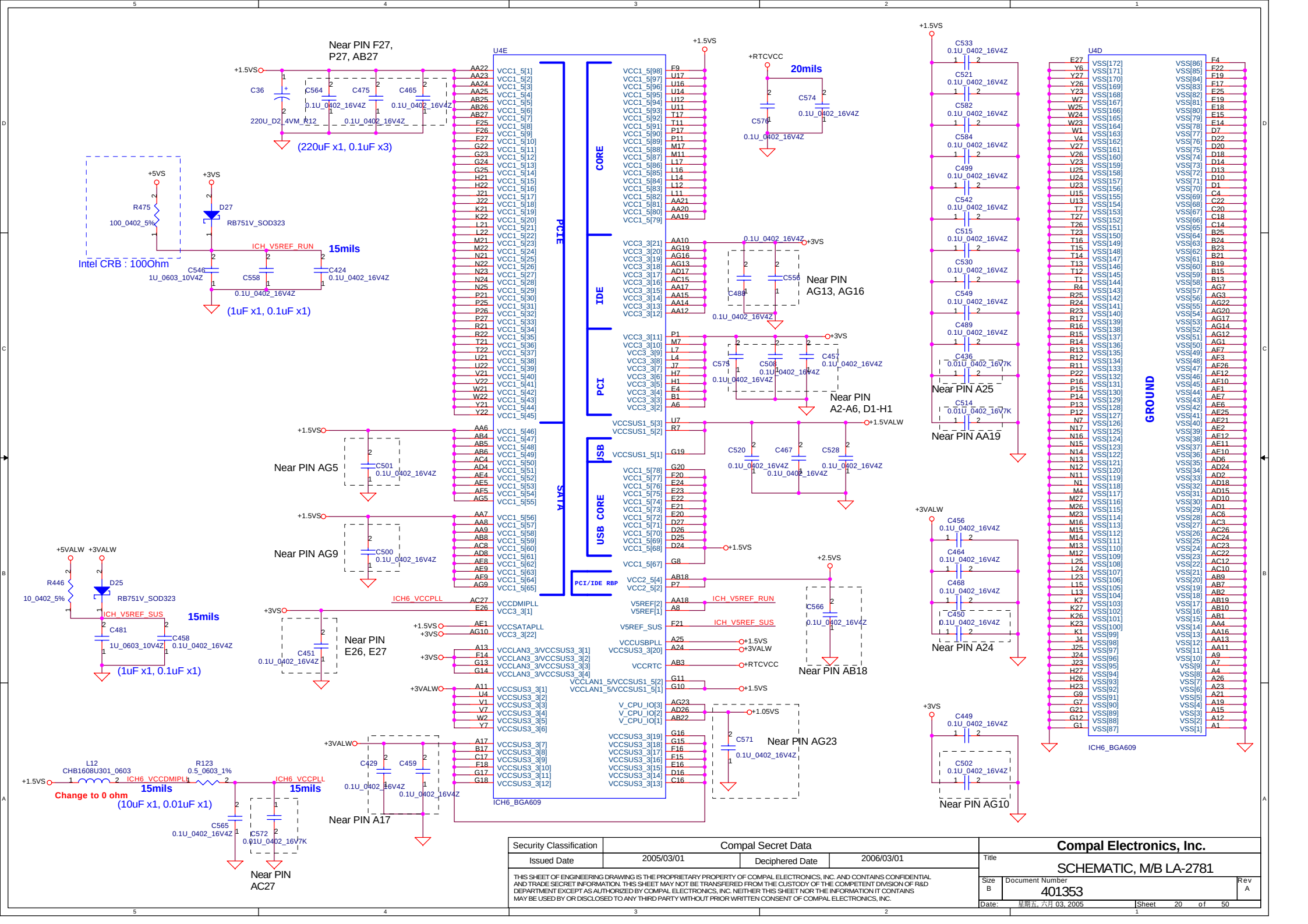
nexaif@hotmail.com



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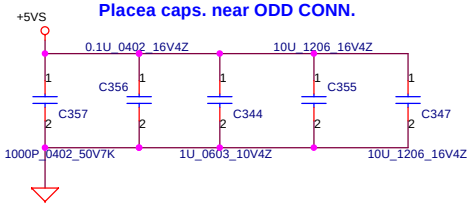
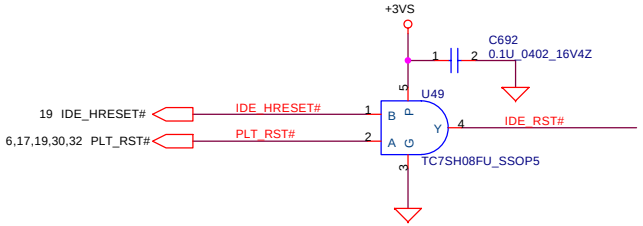
18 IDE_DD[0..15] → IDE_DD[0..15]

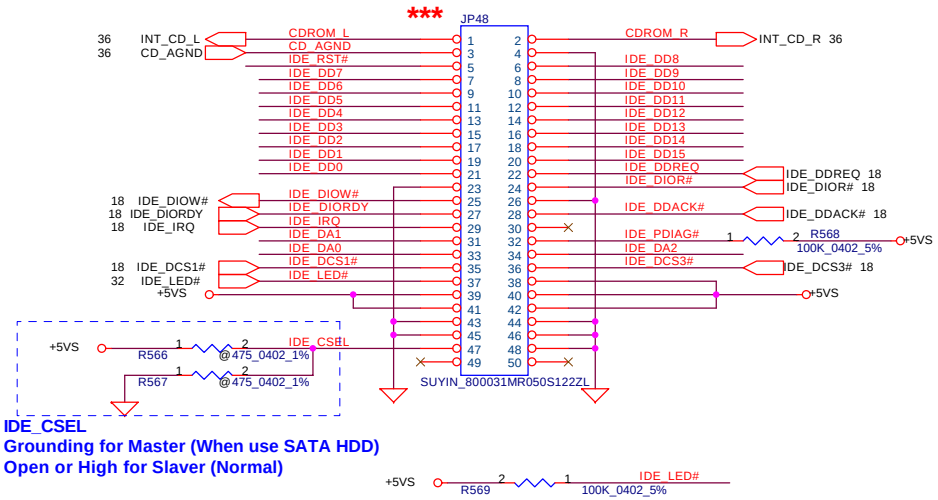
18 IDE_DA[0..2] → IDE_DA[0..2]

Placea caps. near ODD CONN.





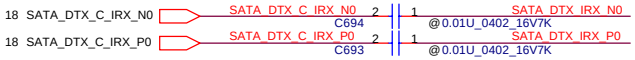
ODD Conn.

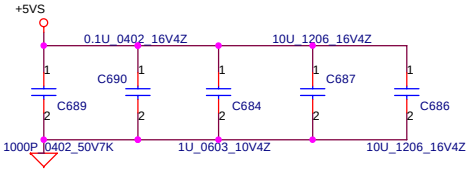


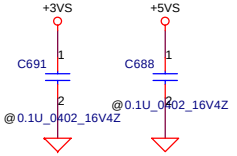
IDE_CSEL
Grounding for Master (When use SATA HDD)
Open or High for Slaver (Normal)

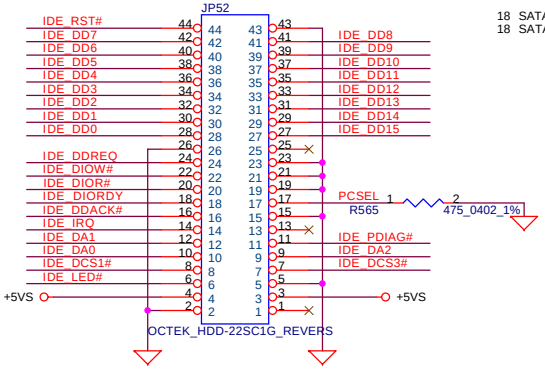
Remove the JP47 and C362,C366,C675,C678,C681

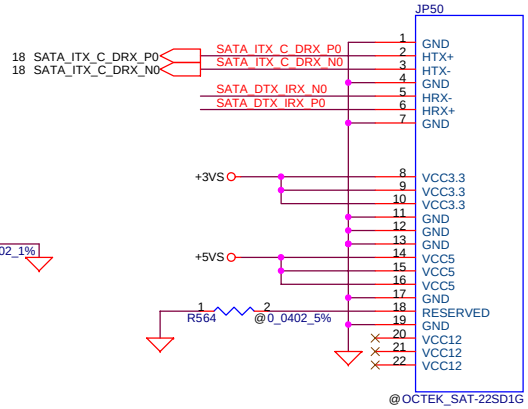
PATA/SATA HDD Conn.











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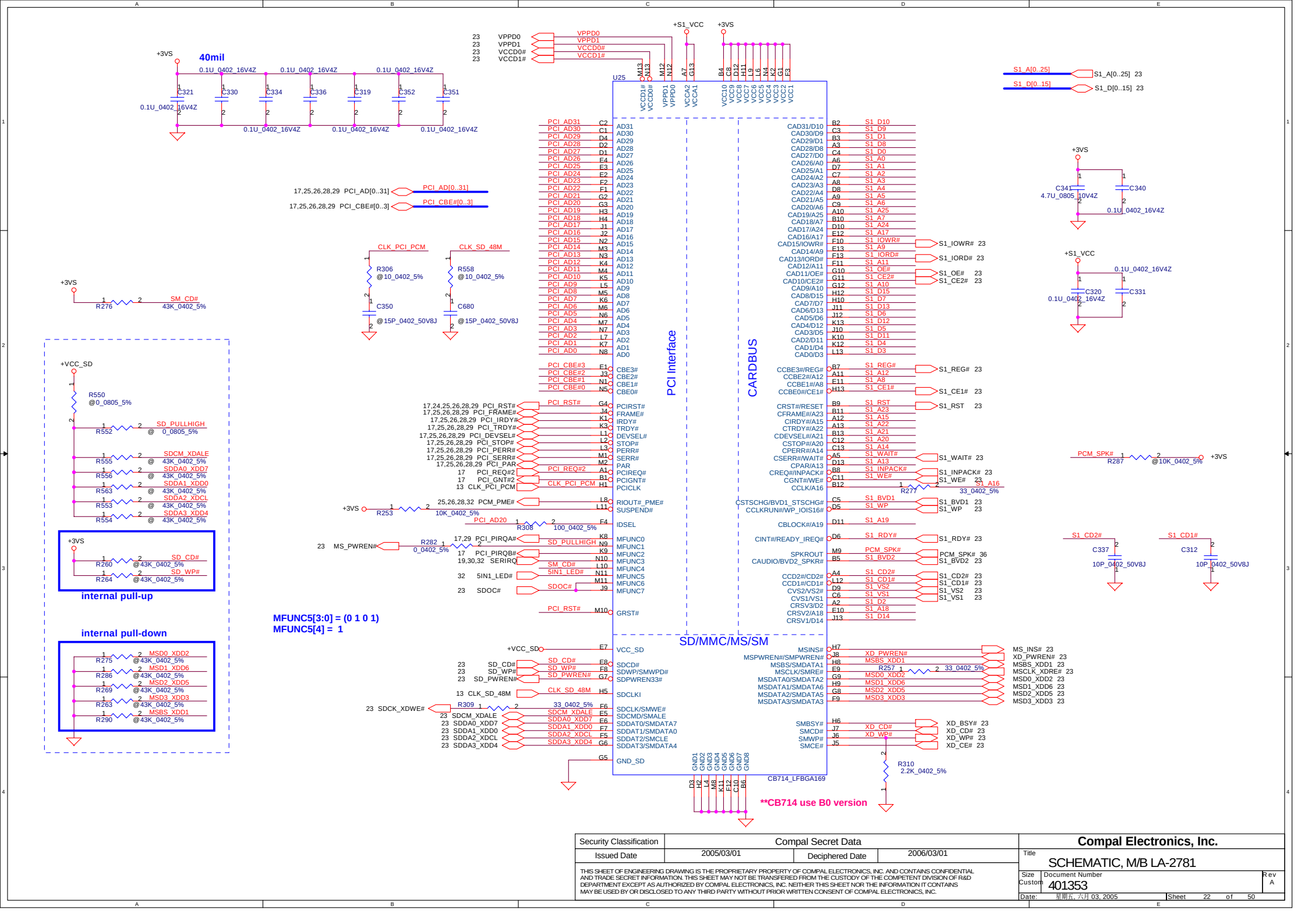

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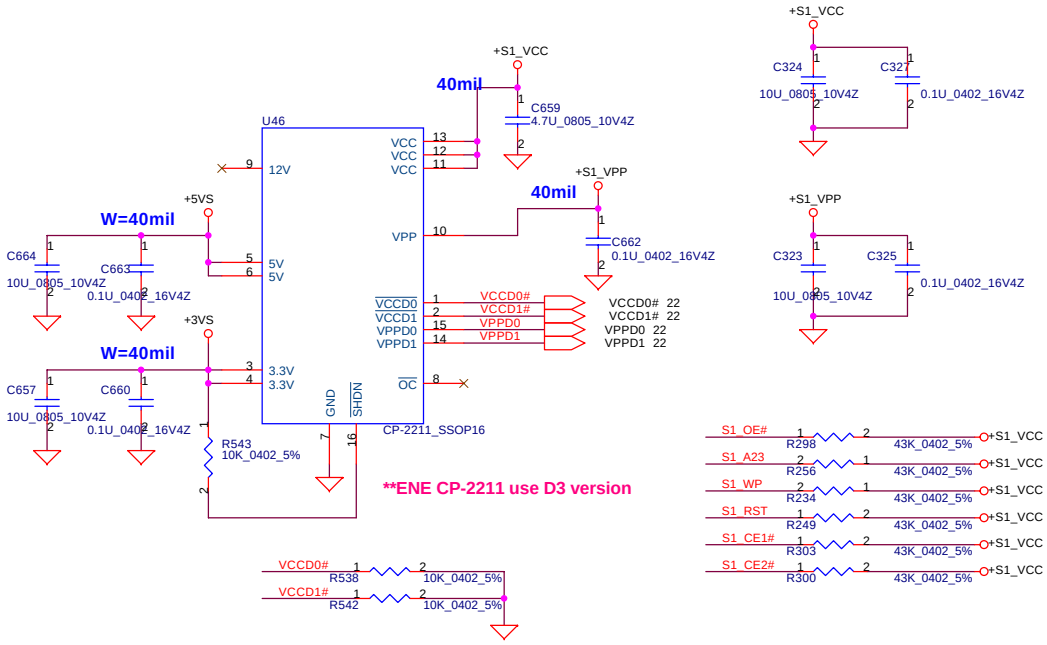
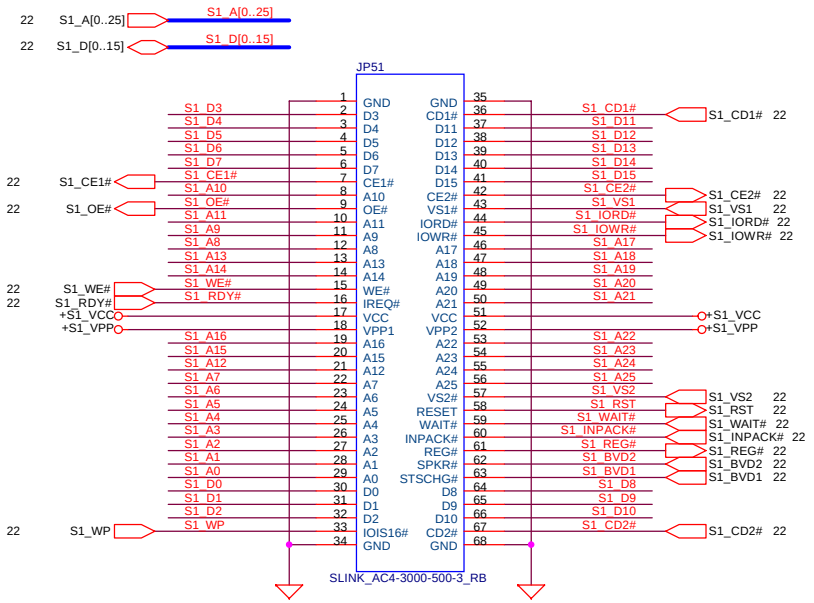
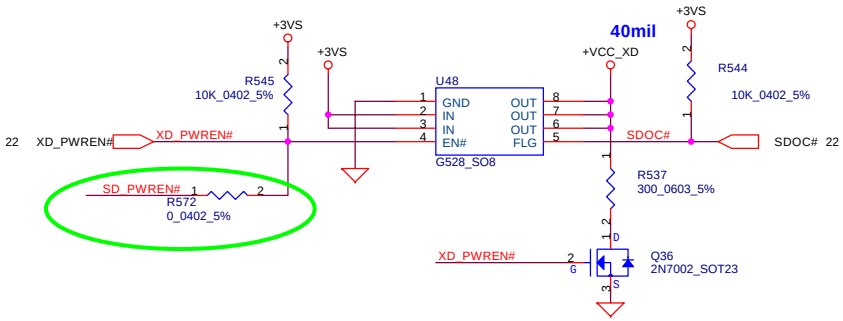
PCMCIA Power Control

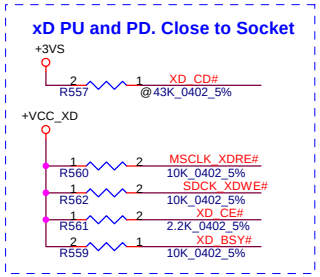


PCMCIA Socket

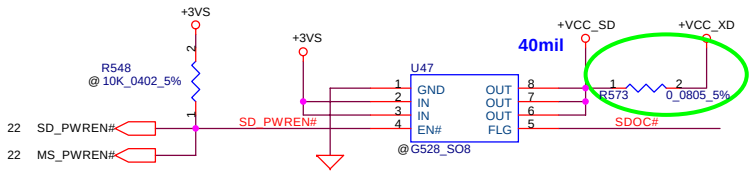


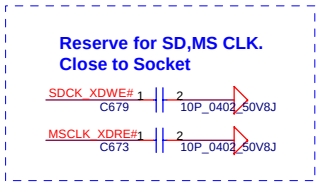
XD Power Control

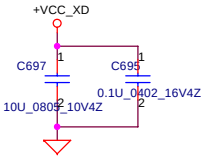


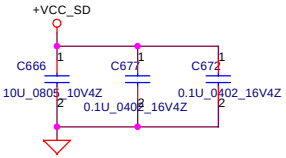


SD/MS Power Control

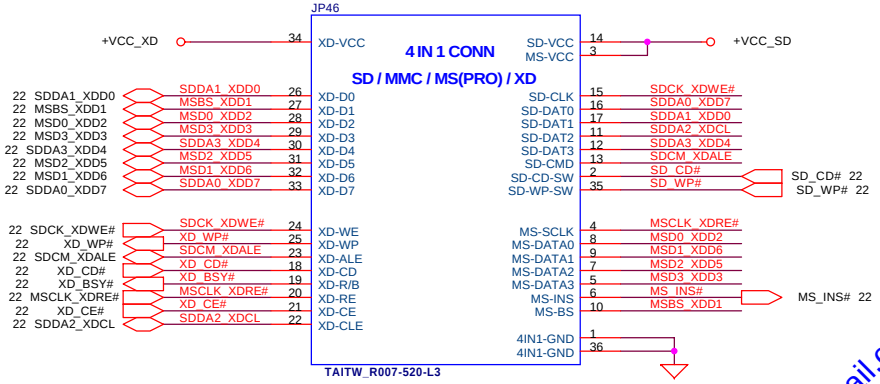








4 IN 1 Socket



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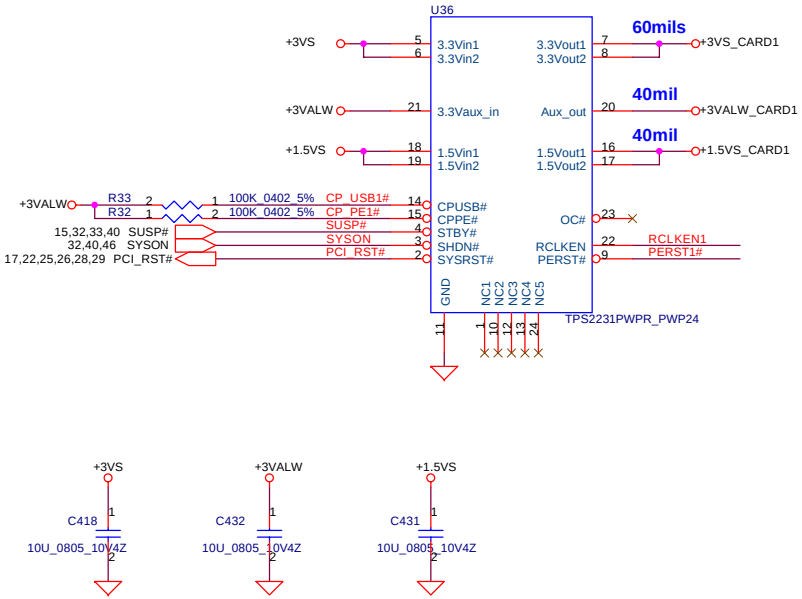
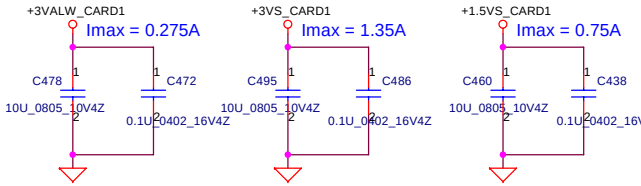
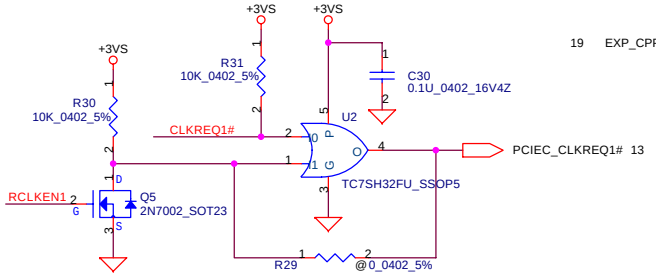
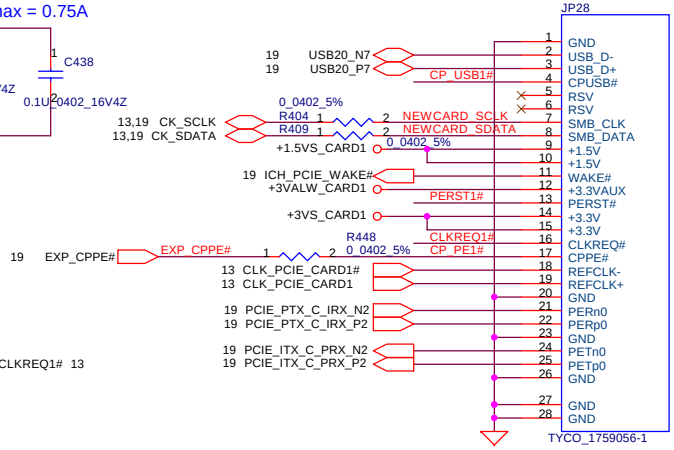
New Card Power Switch







New Card Socket (Left)



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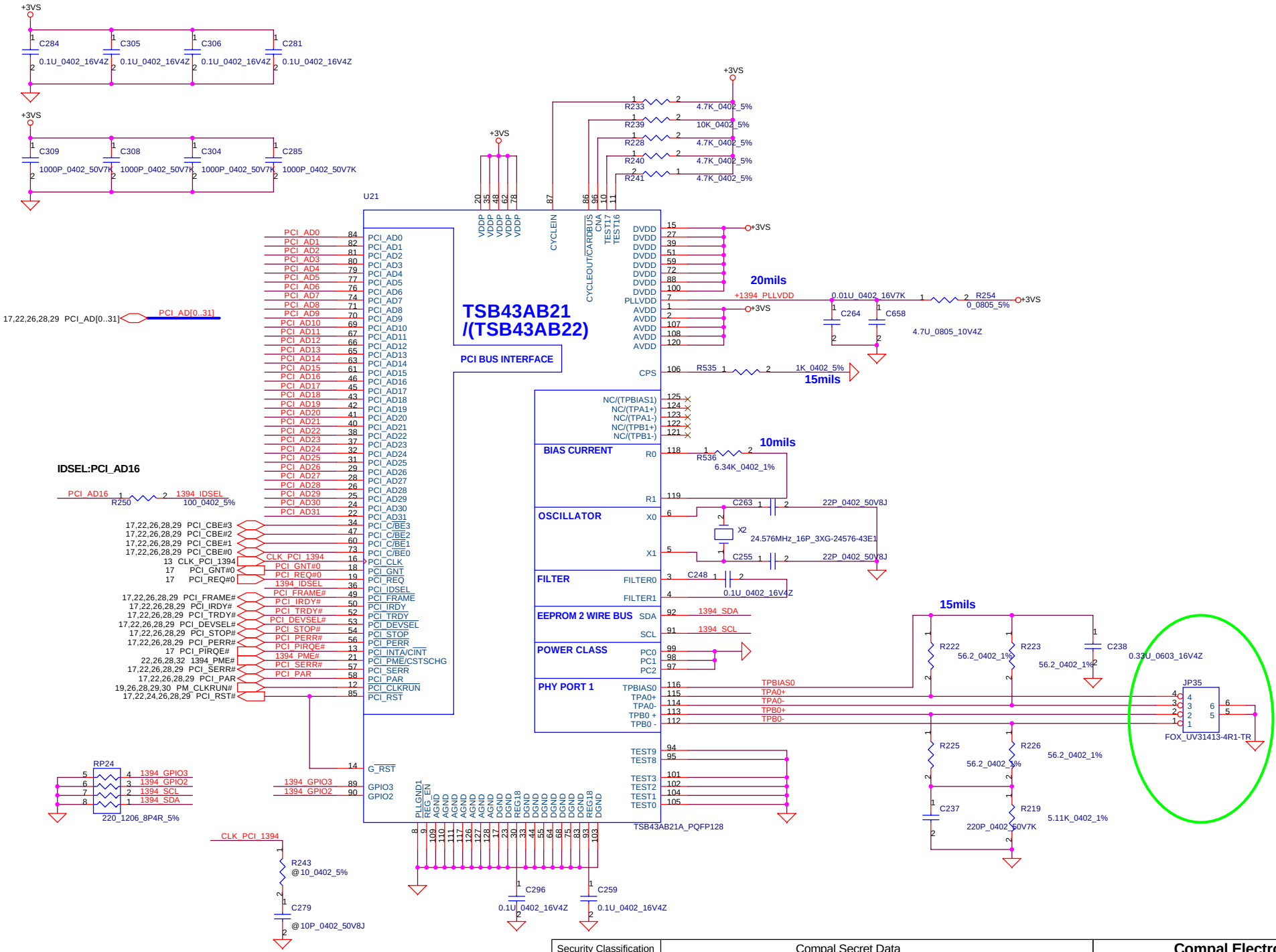

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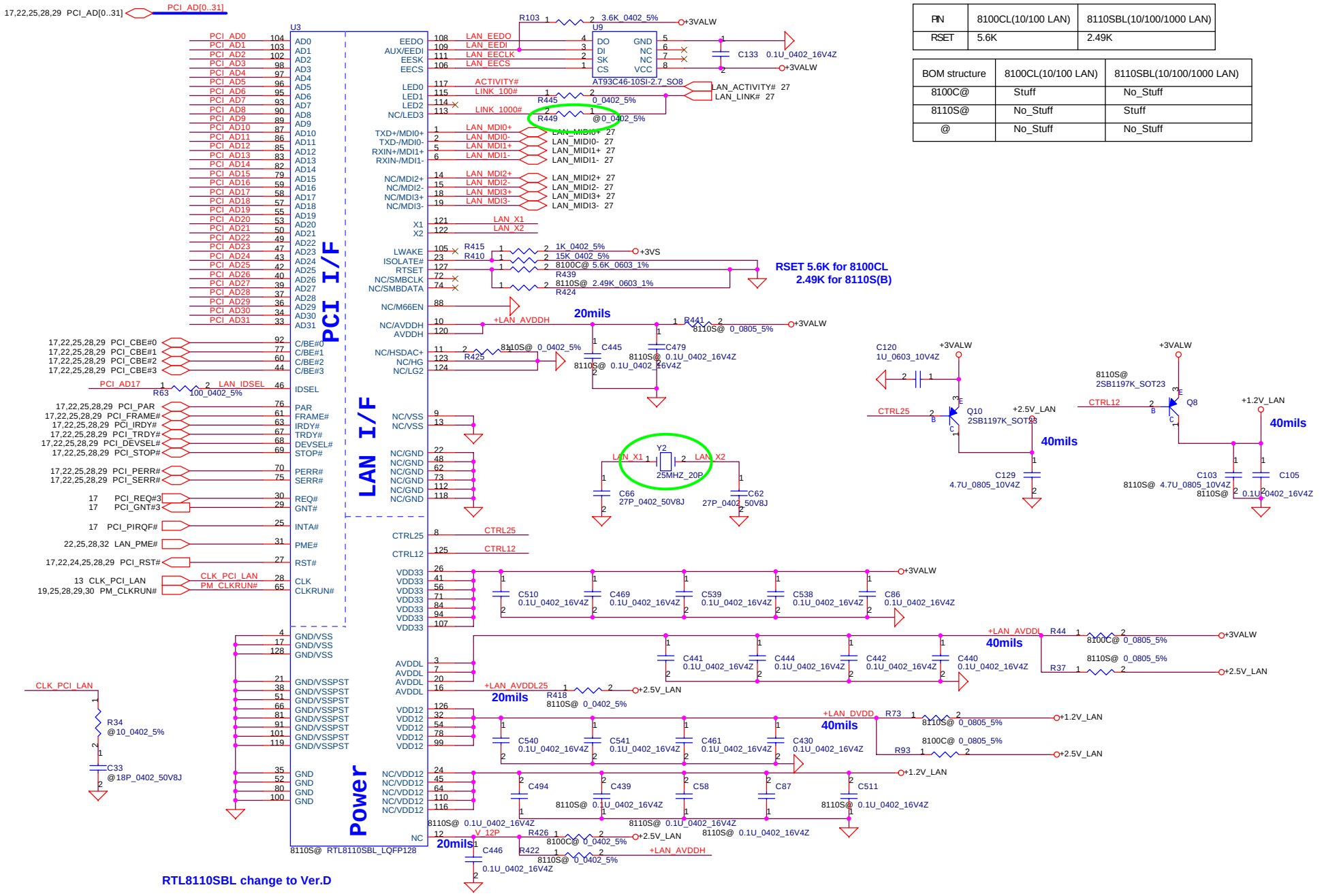

PIN	8100CL(10/100 LAN)	8110SBL(10/100/1000 LAN)
RSET	5.6K	2.49K

BOM structure	8100CL(10/100 LAN)	8110SBL(10/100/1000 LAN)
8100C@	Stuff	No_Stuff
8110S@	No_Stuff	Stuff
@	No_Stuff	No_Stuff

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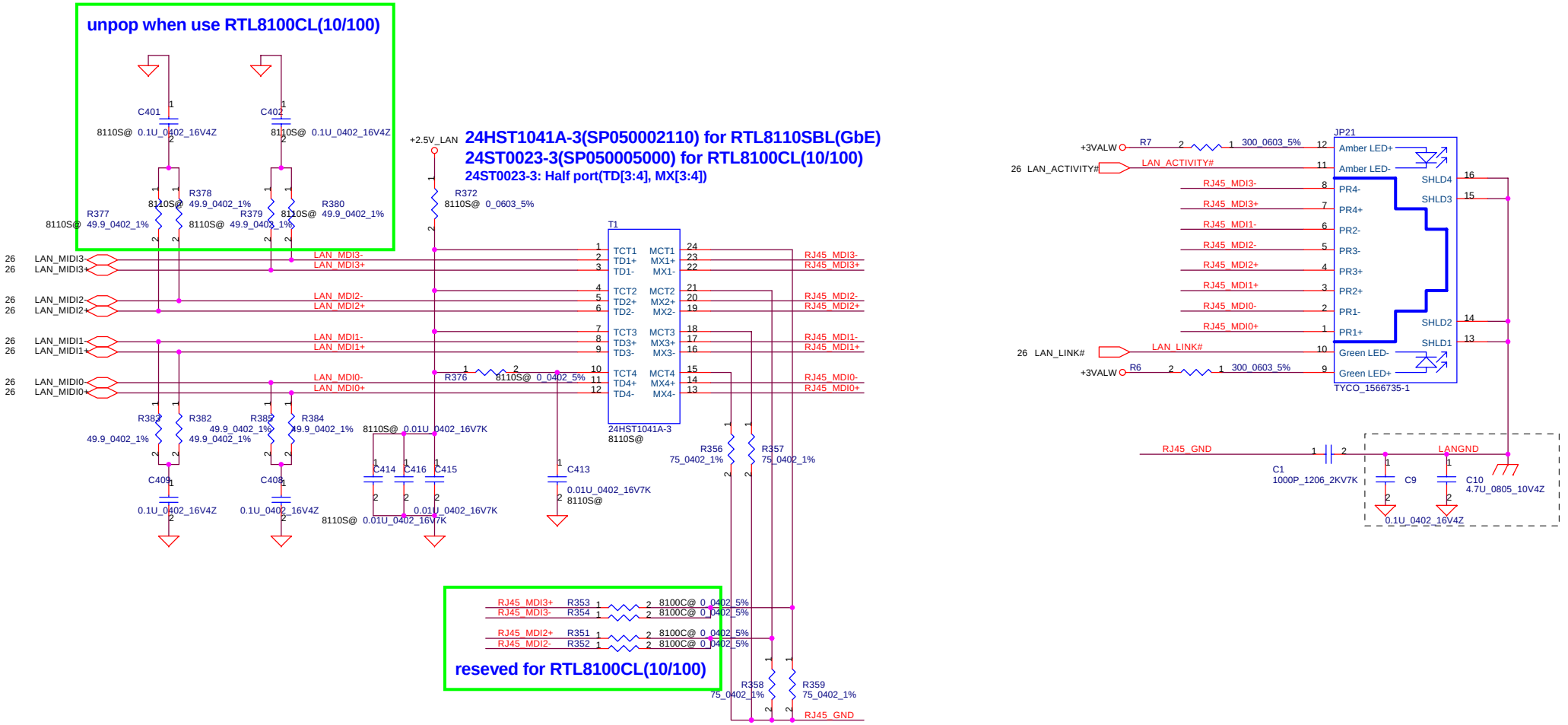
LAN RTL8110SBL/RTL8100CL



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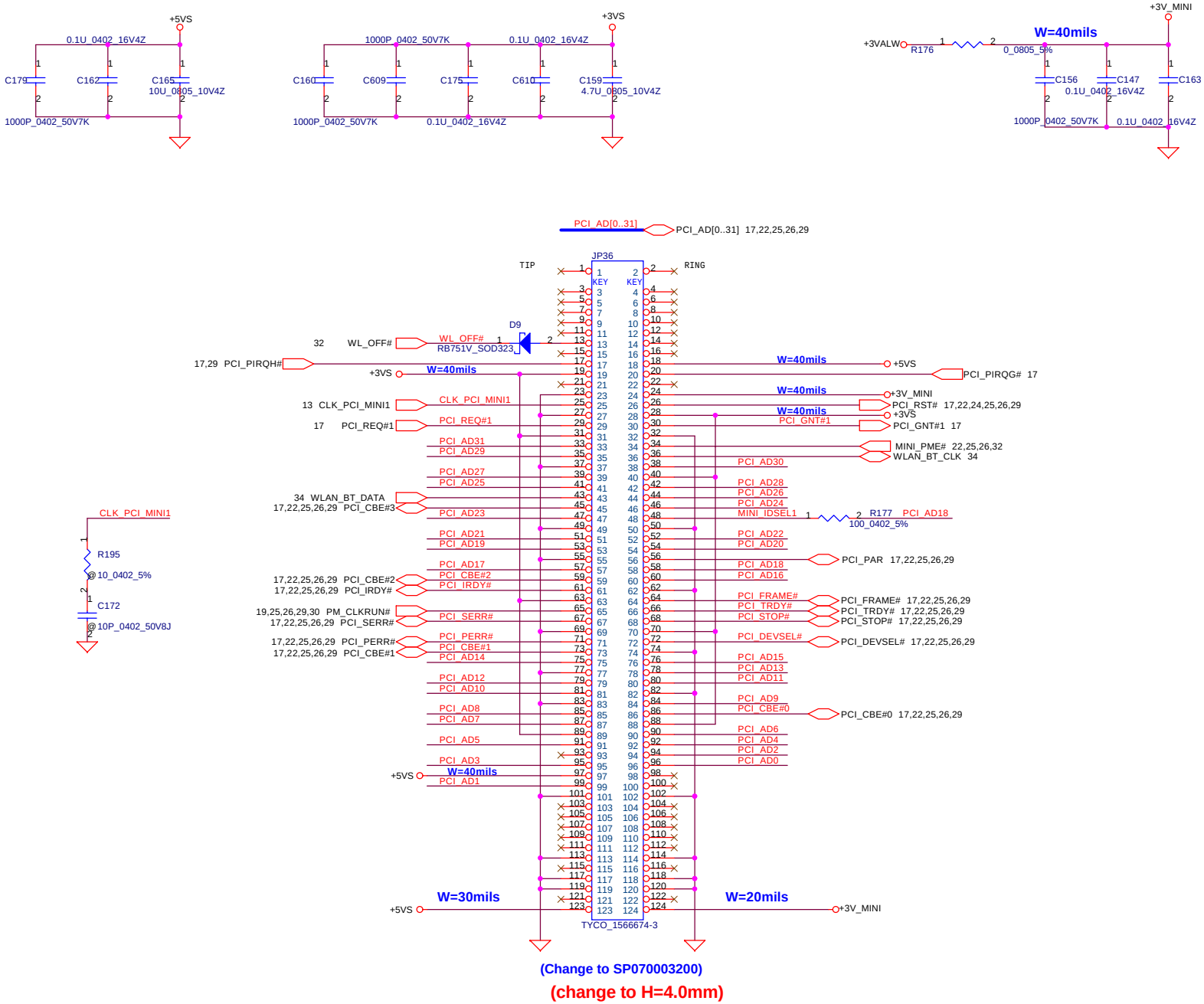

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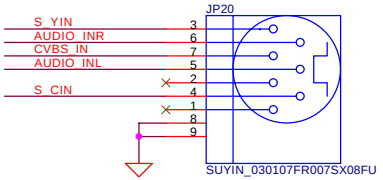
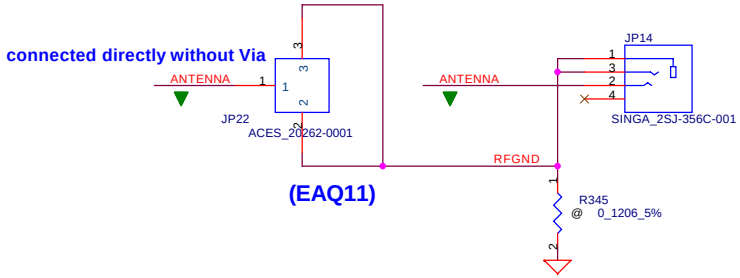
TV-Tuner

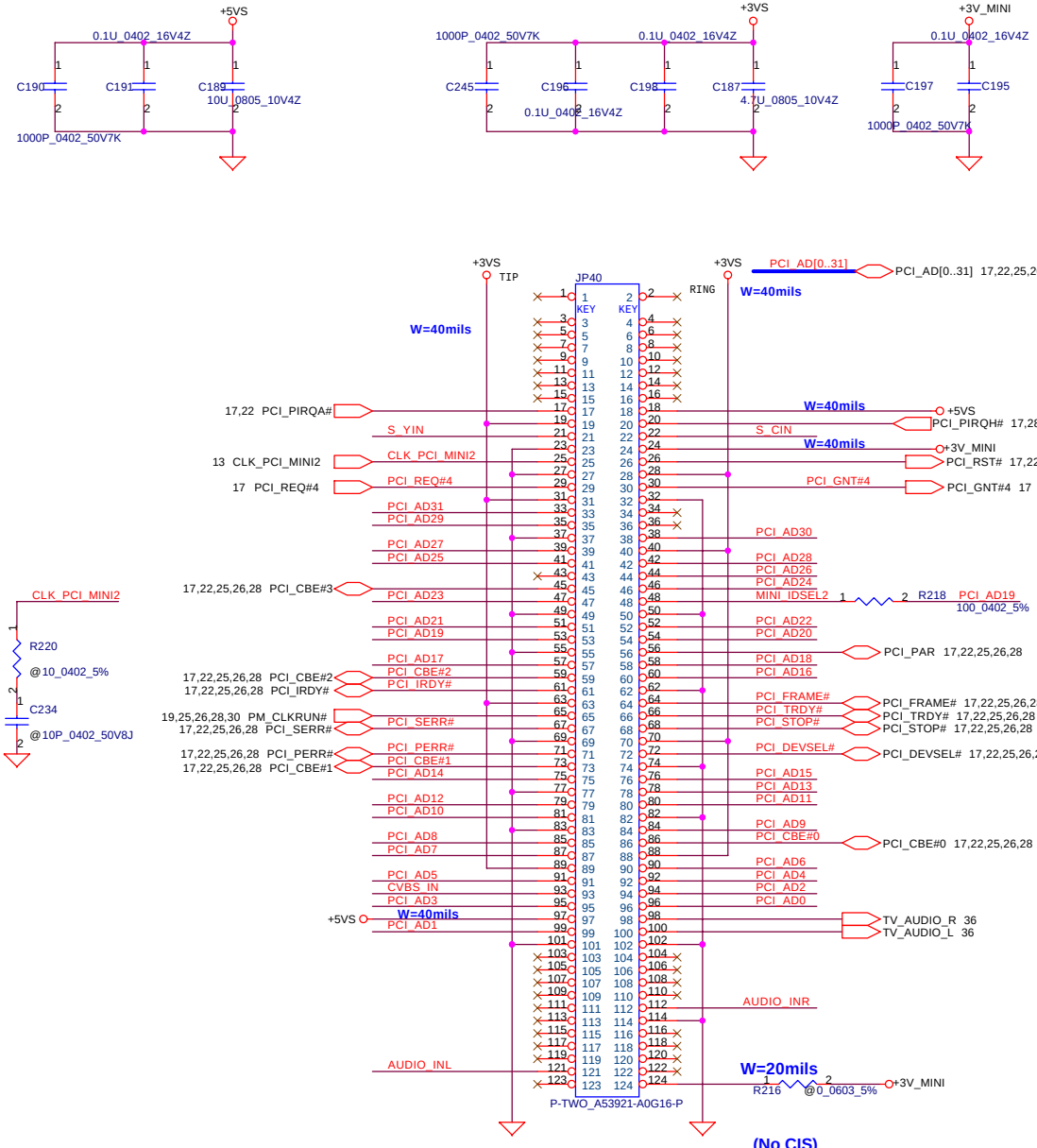
AV In



Acer TV-Tuner Design Guide Rev1.1
1. N/A
2. N/A
3. S-Video - Y
4. S-Video - C
5. Audio - Left
6. Audio - Right
7. CVBS

RF In





(EDL71 pin define)

(No CIS)

(For TV-Tuner change to H=9.2mm)

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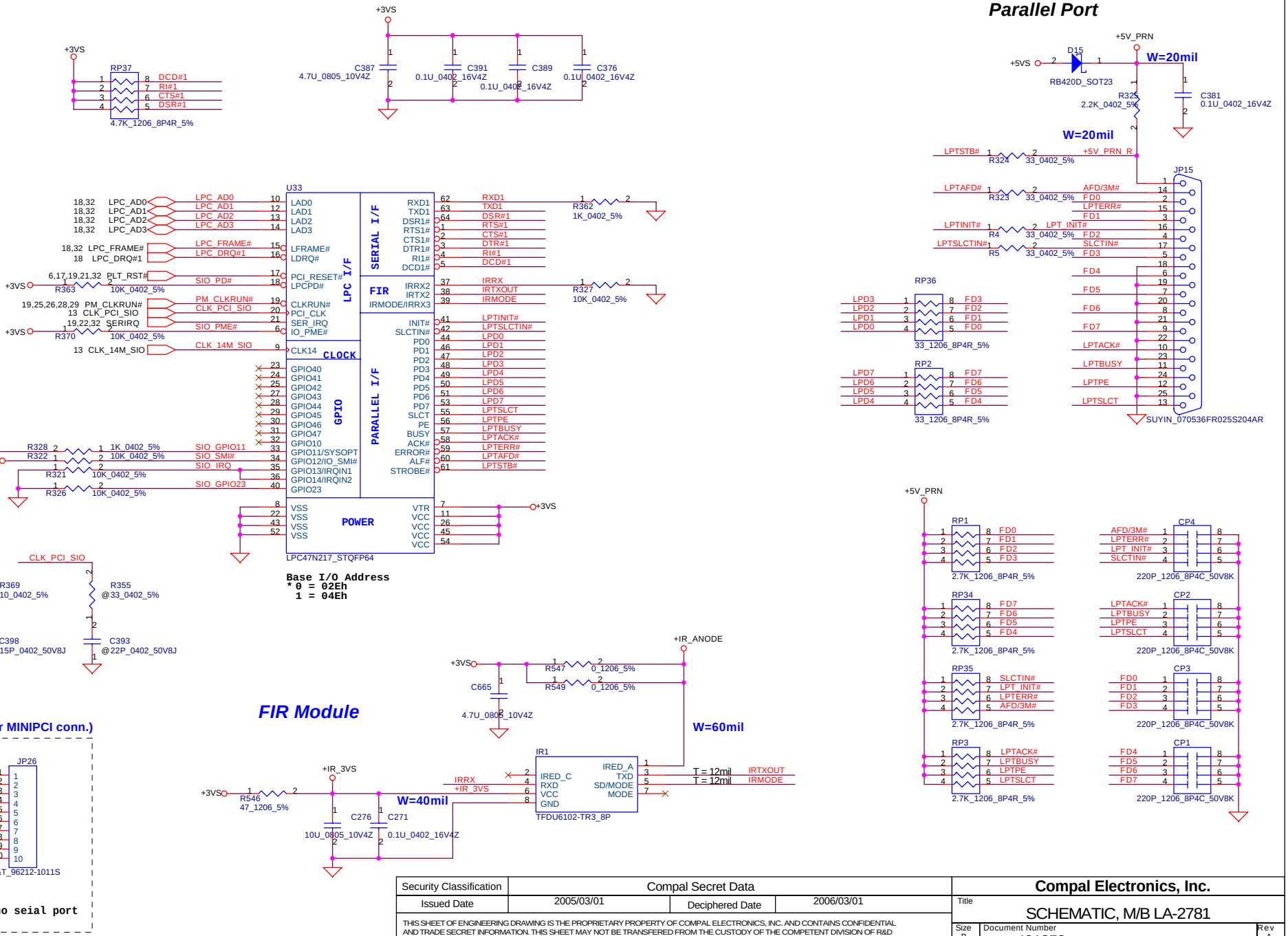
SUPER I/O SMsC LPC47N217



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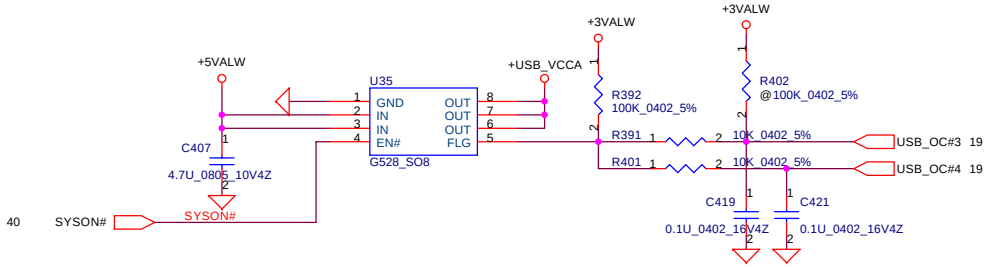

USB CONN. 1 & 2

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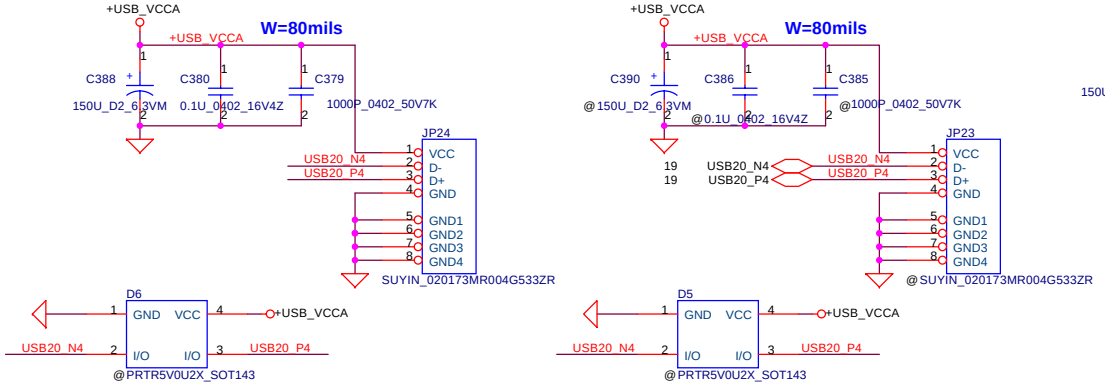
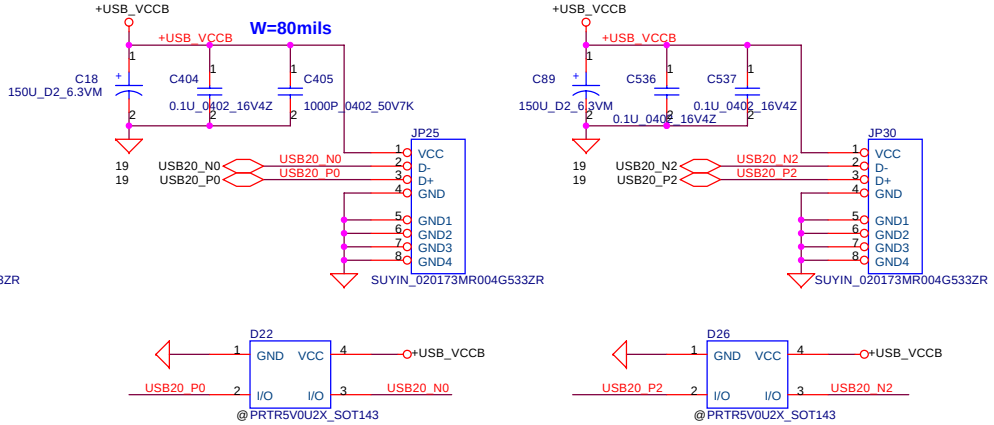


USB CONN. 3 & 5

(Place on the right side)



USB CONN. 5

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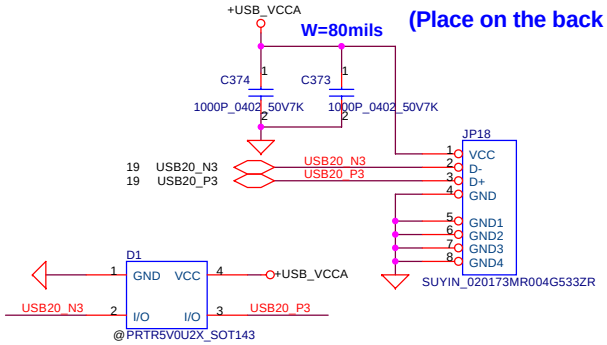

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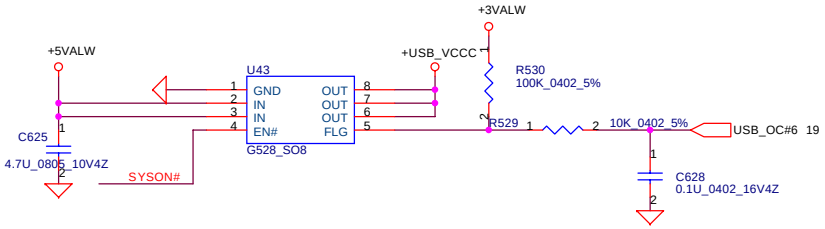

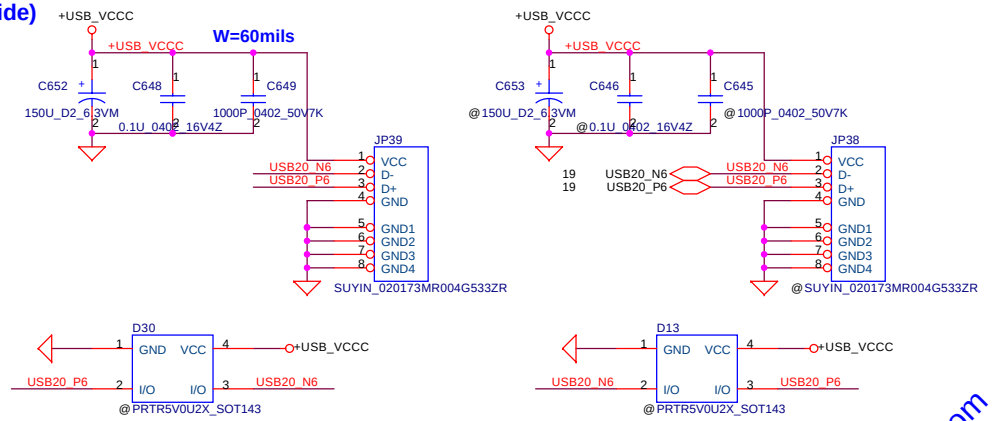

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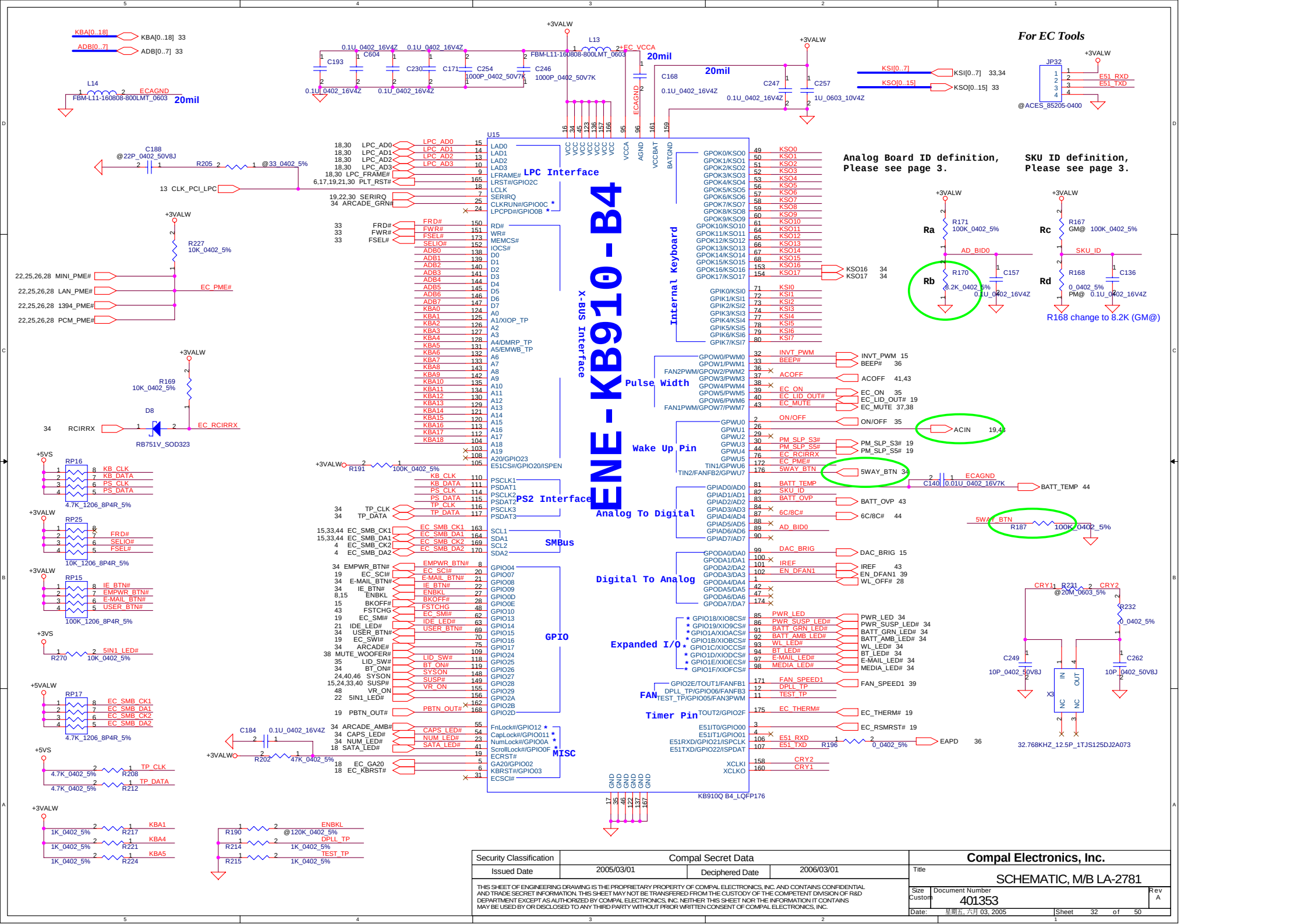

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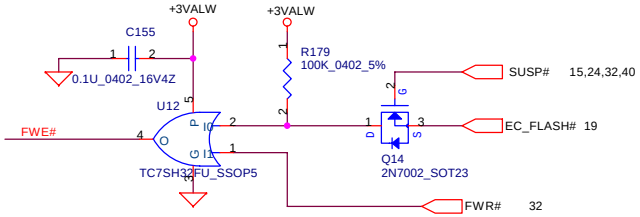
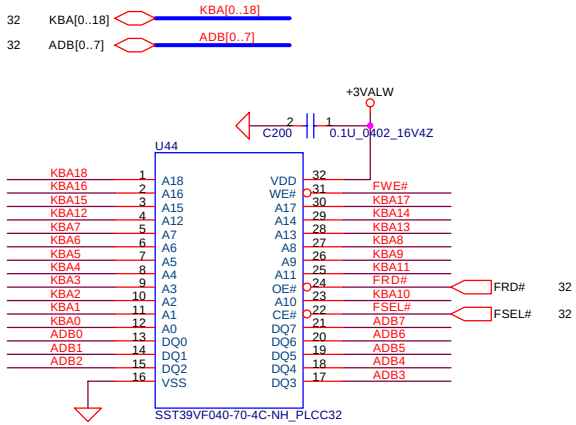
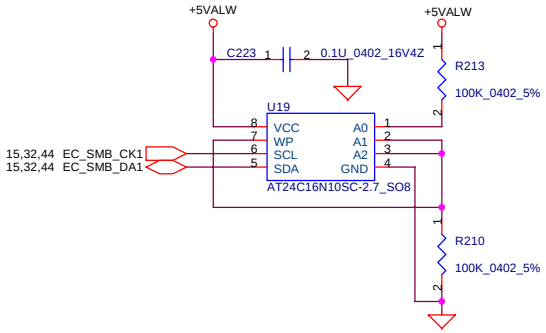
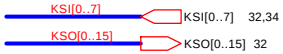


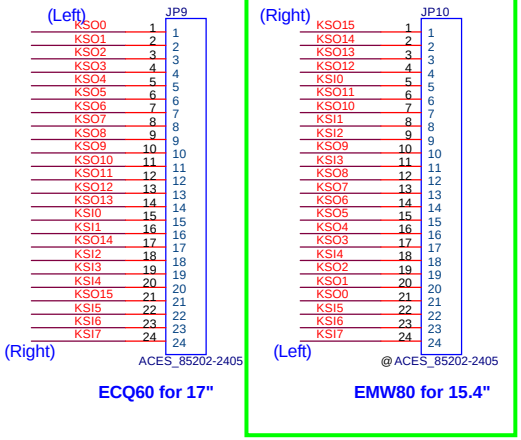
512KB Flash ROM

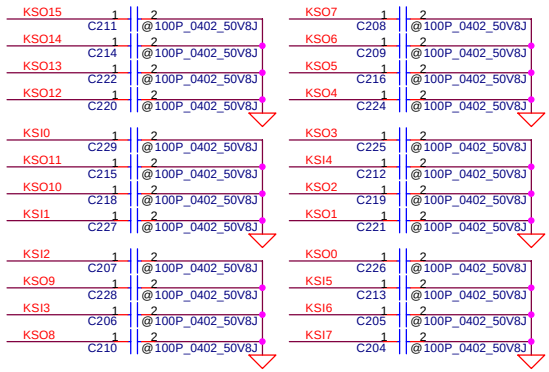




INT_KBD Conn.







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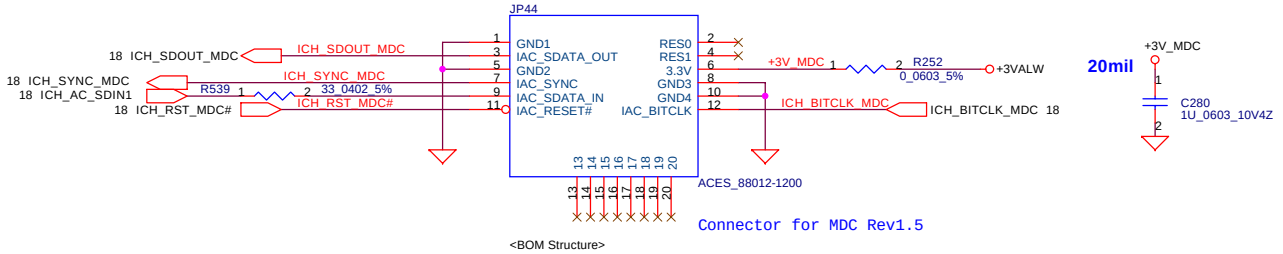
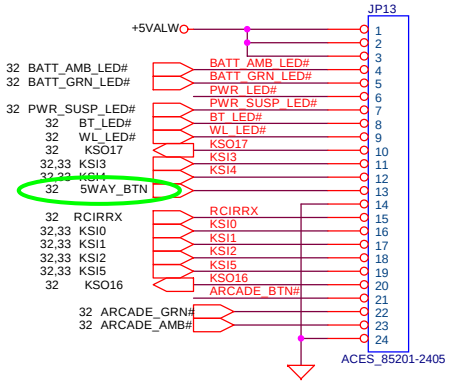
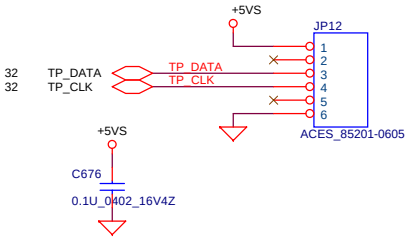
MDC Conn.



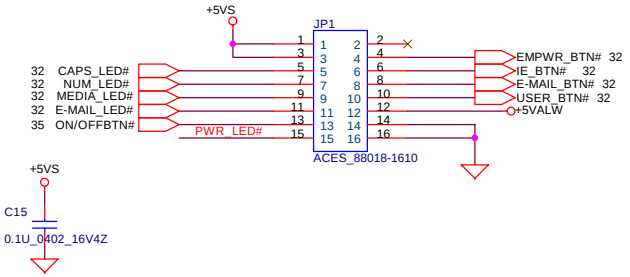
To Media/B Conn.

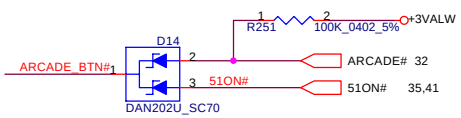


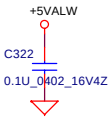
To TP/B Conn.

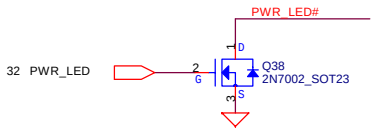


To LED/B Conn.



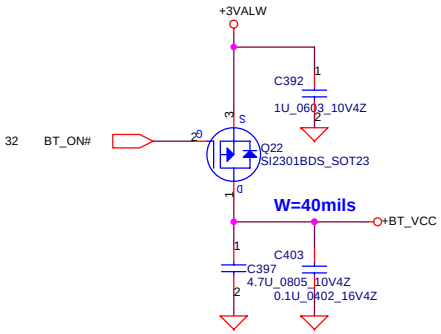


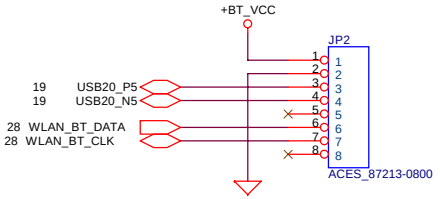




	KSO16	KSO17
KSI0	VOL_UP	LEFT
KSI1	RIGHT	VOL_DOWN
KSI2	PLAY	ENTER
KSI3	STOP	BT_EN#
KSI4	REV	WL_EN#
KSI5	NEXT	

Bluetooth Conn.





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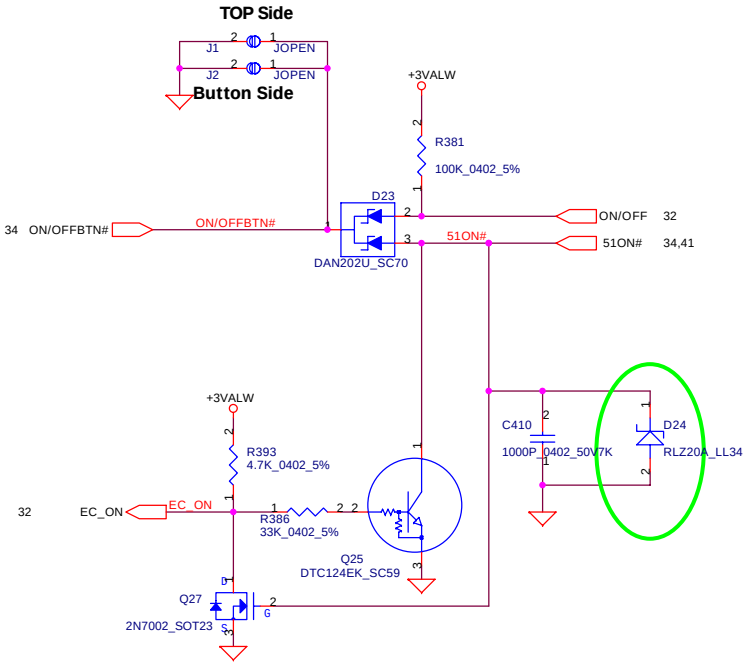
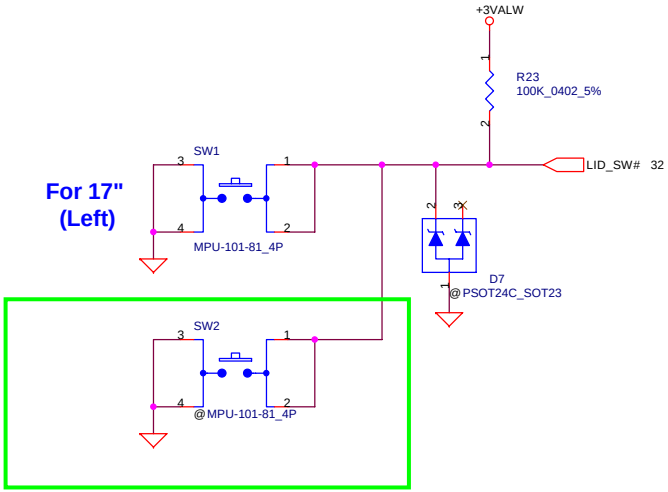
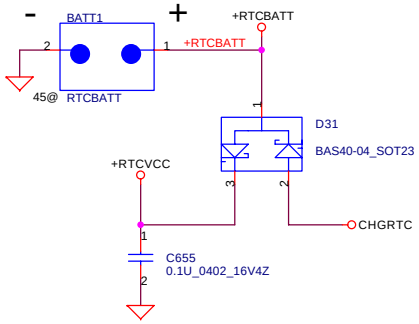
ON/OFF switch



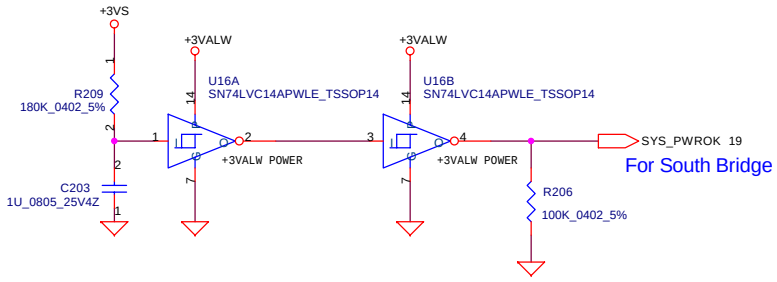
Lid Switch

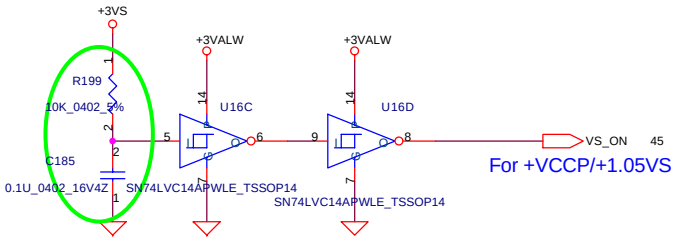


RTC Battery



Power ON Circuit





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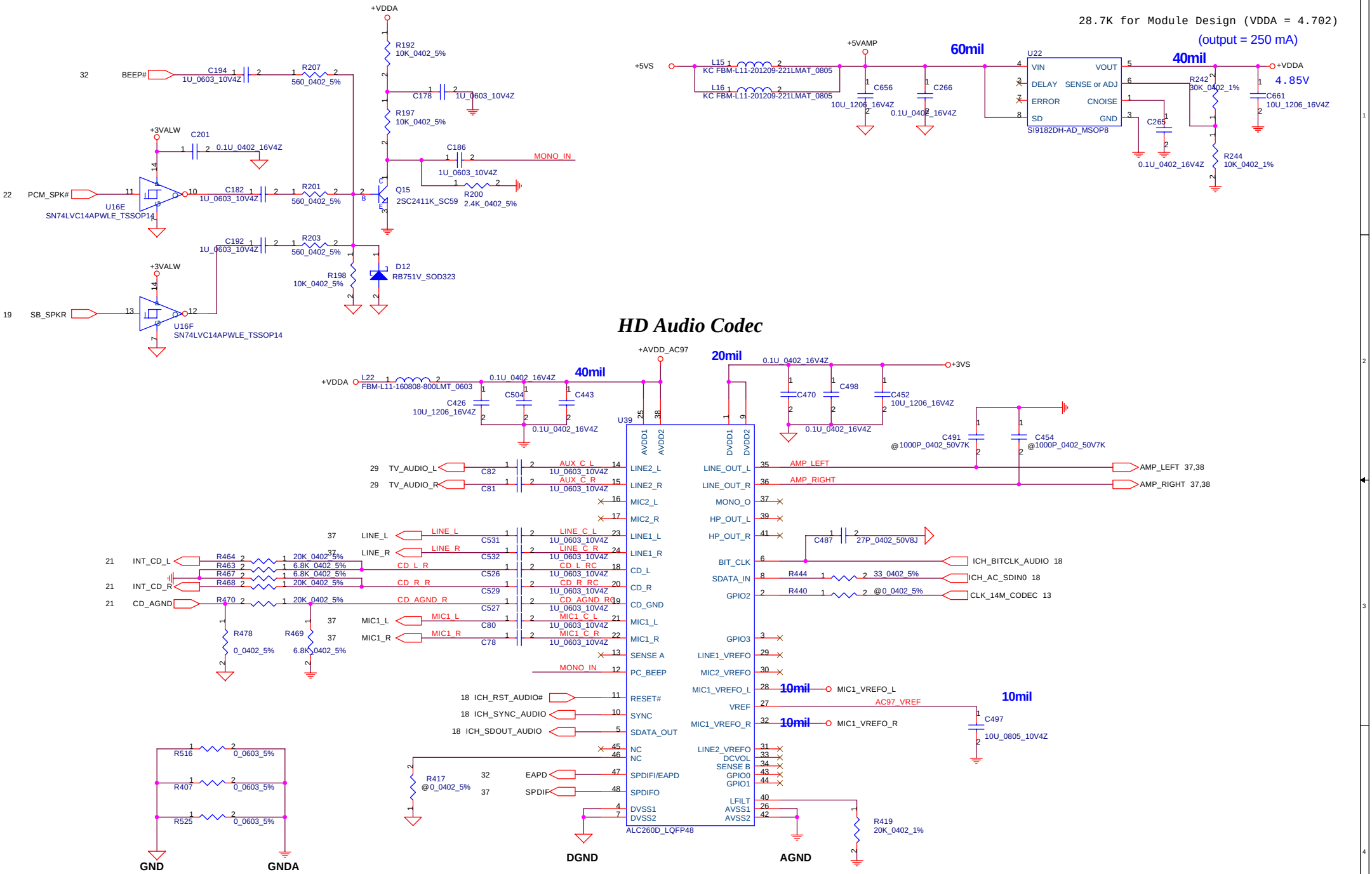
28.7K for Module Design (VDDA = 4.702)
(output = 250 mA)

HD Audio Codec



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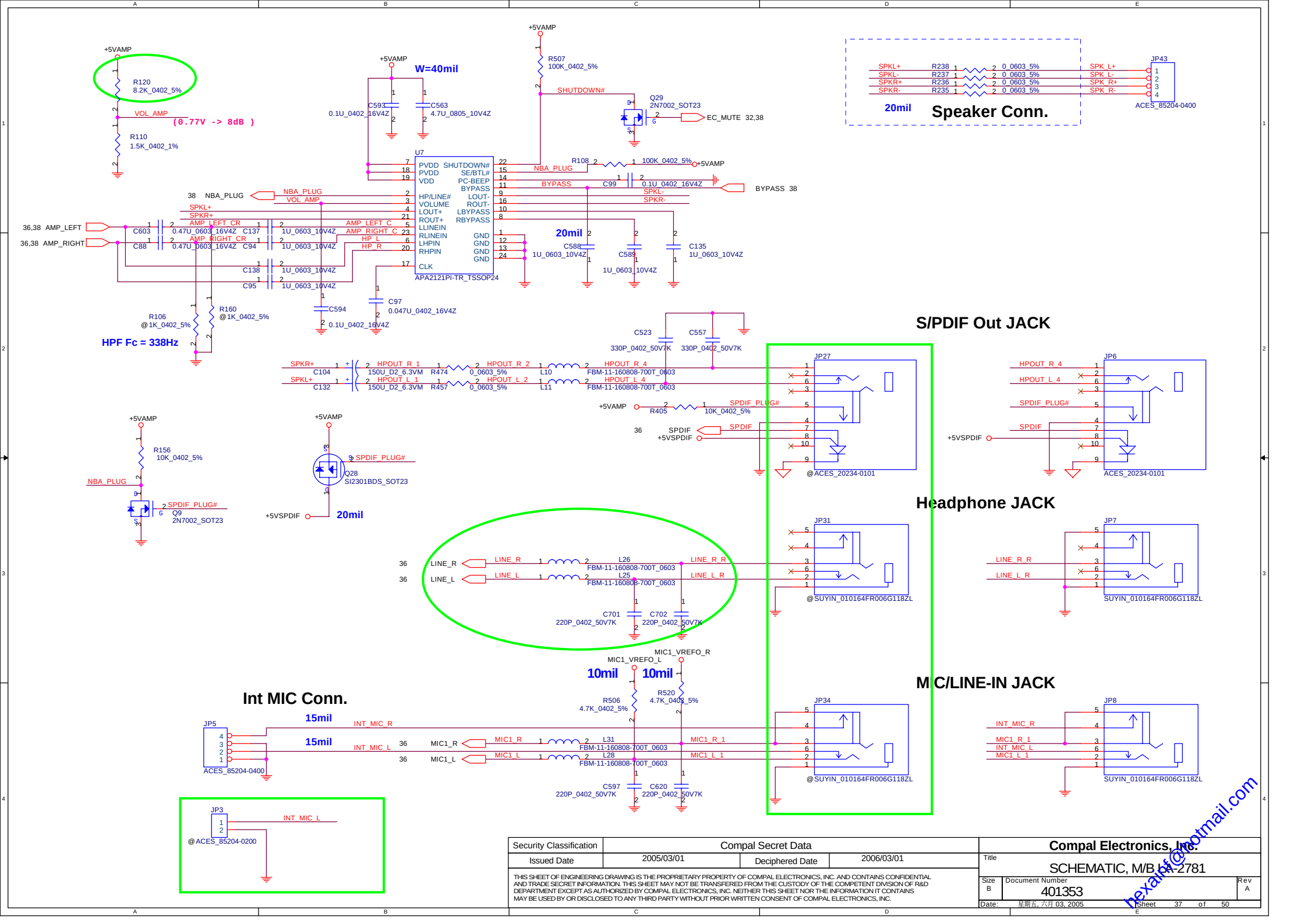

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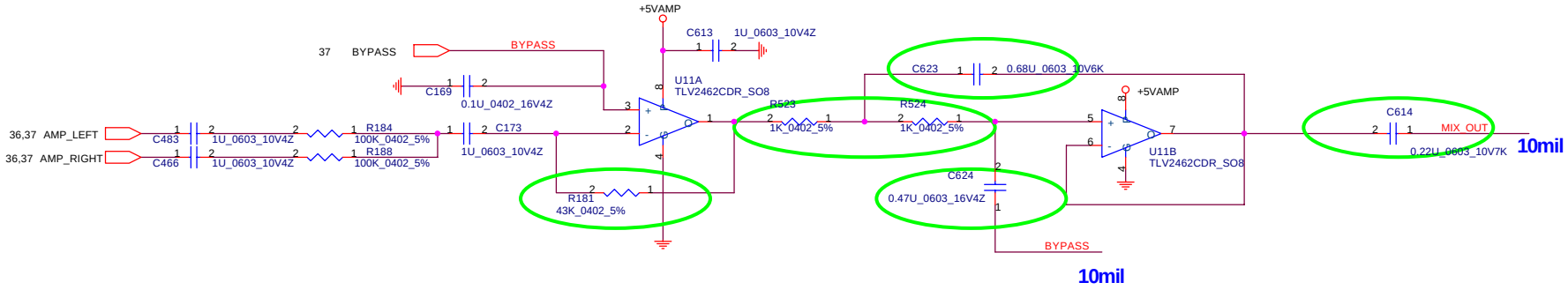
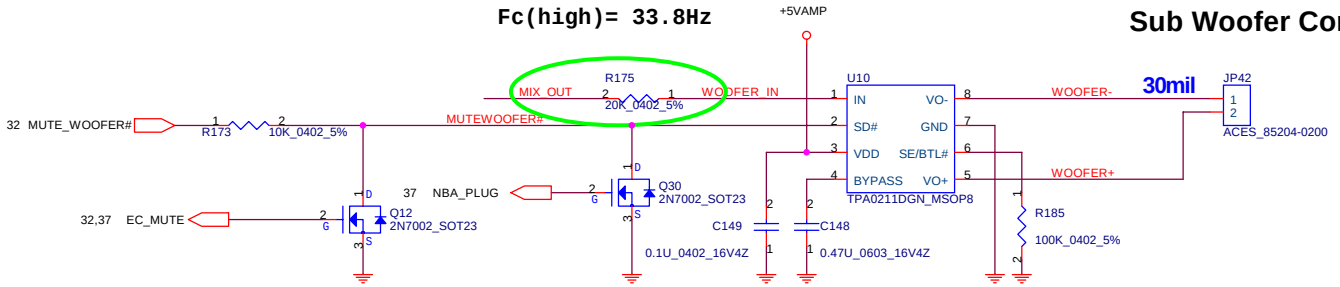


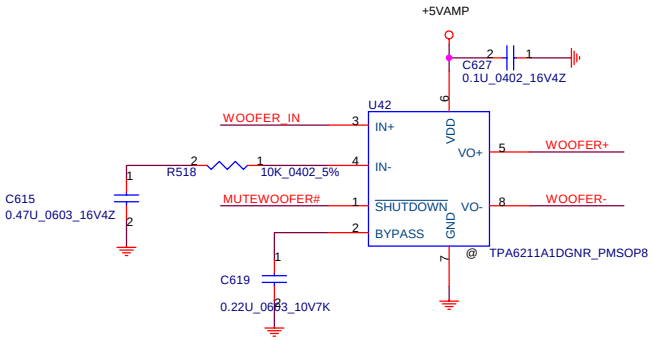
10mil

fo= 725 Hz

Fc(high)= 33.8Hz

Sub Woofer Conn.





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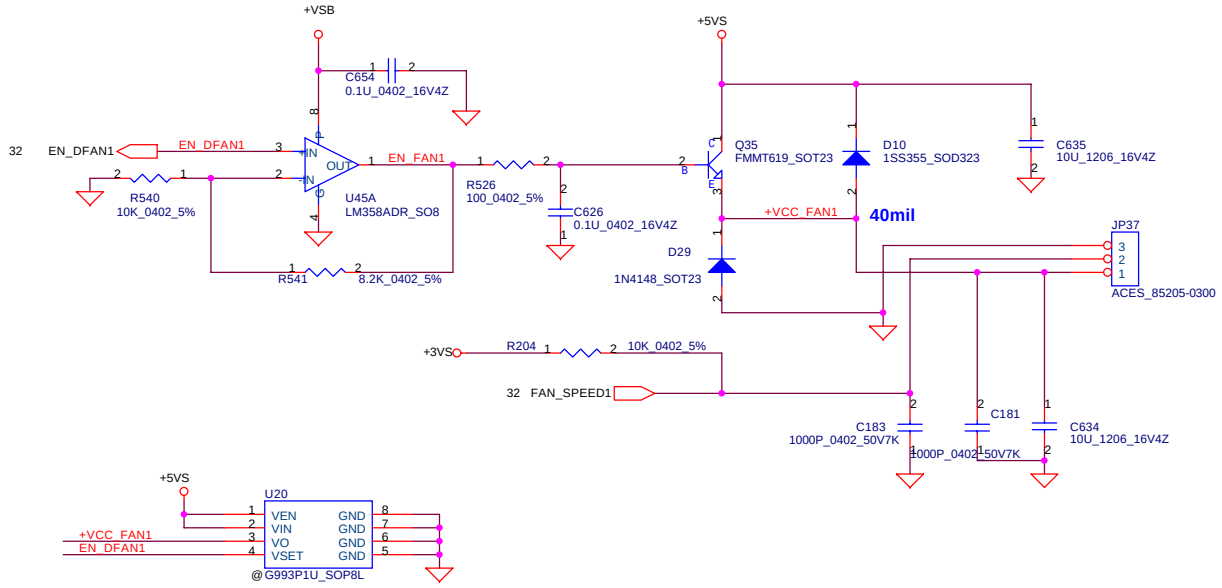
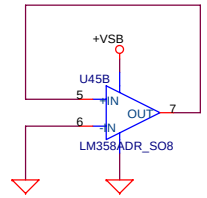
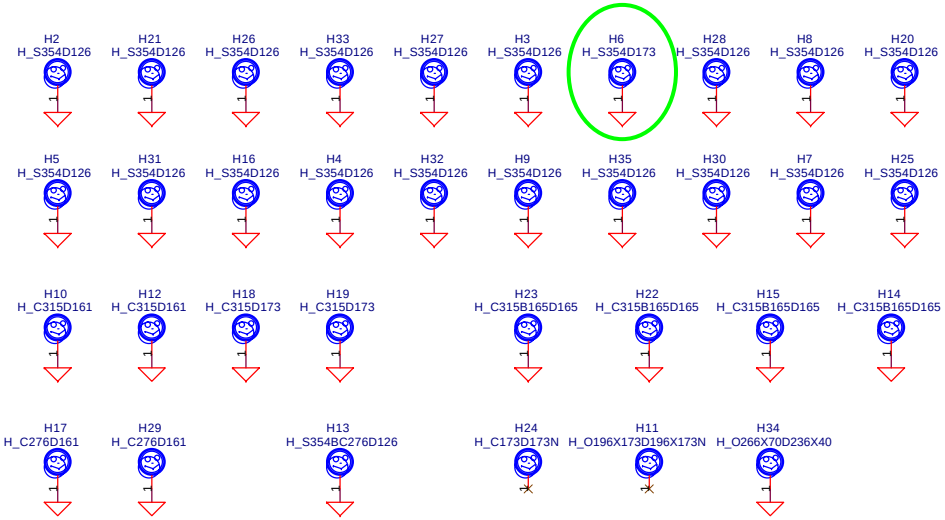
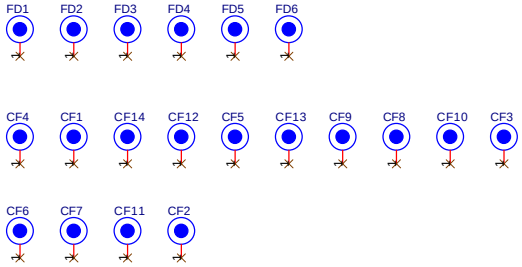
FAN Conn









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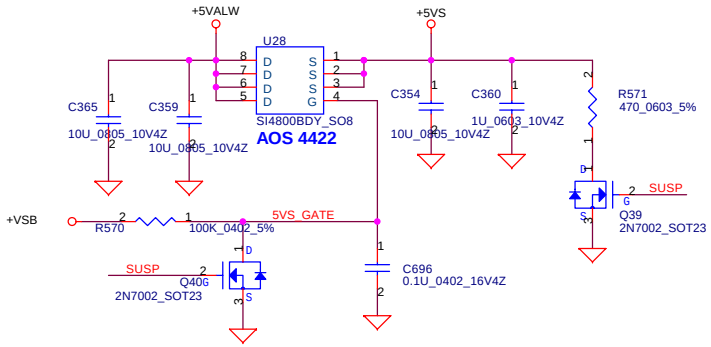
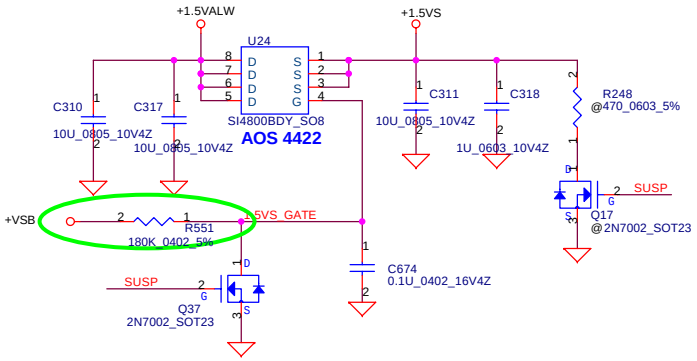
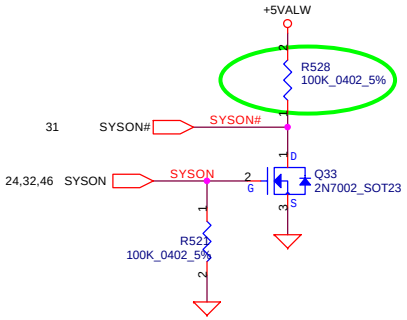
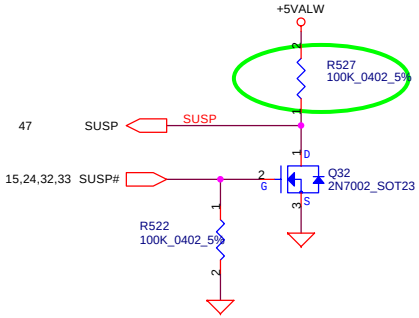
+5VALW TO +5VS



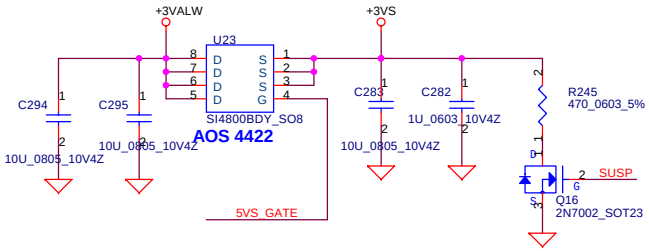
+1.5VALW TO +1.5VS



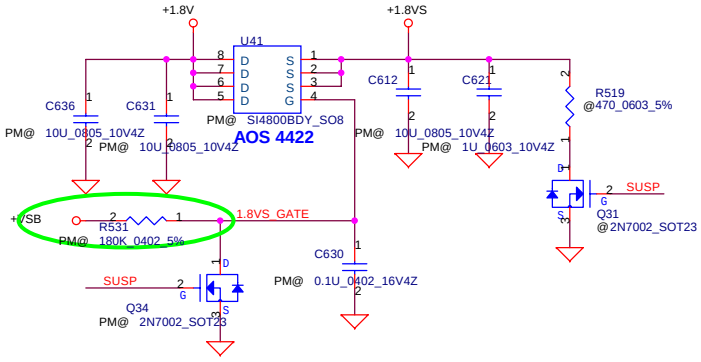




+3VALW TO +3VS



+1.8V to +1.8VS



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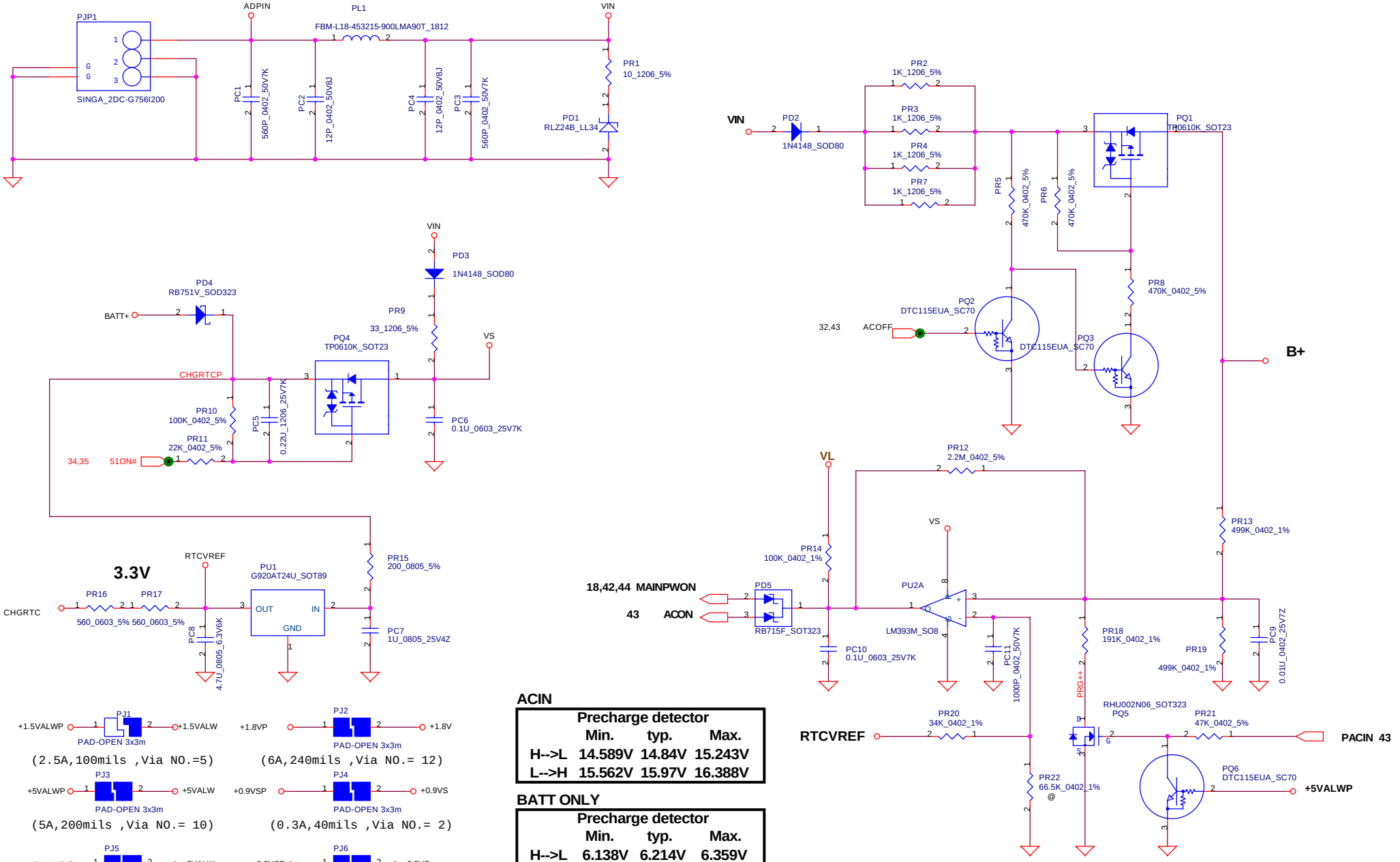

ACIN

Precharge detector	Min.	typ.	Max.
H-->L	14.589V	14.84V	15.243V
L-->H	15.562V	15.97V	16.388V

BATT ONLY

Precharge detector	Min.	typ.	Max.
H-->L	6.138V	6.214V	6.359V
L-->H	7.196V	7.349V	7.505V

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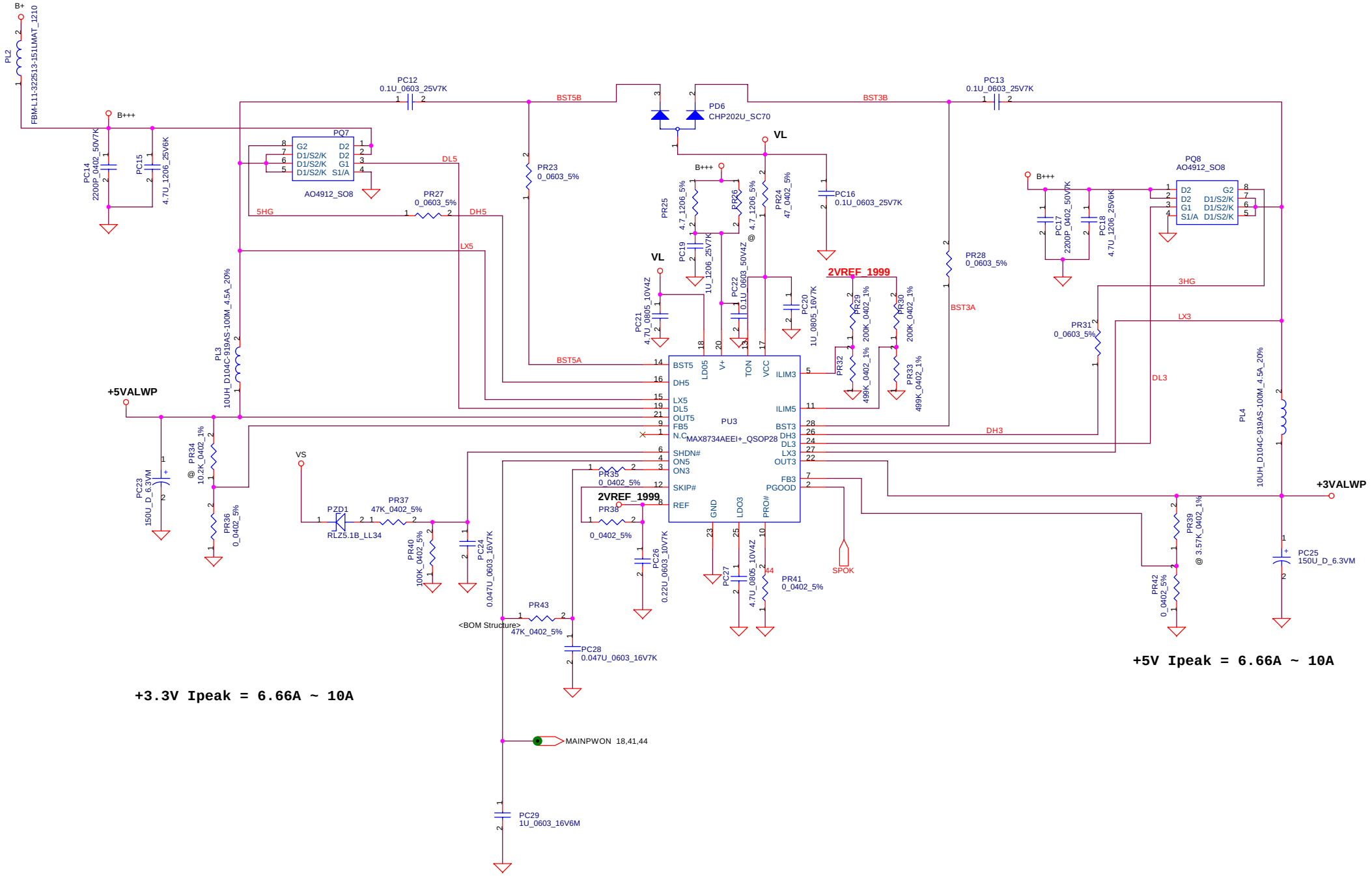

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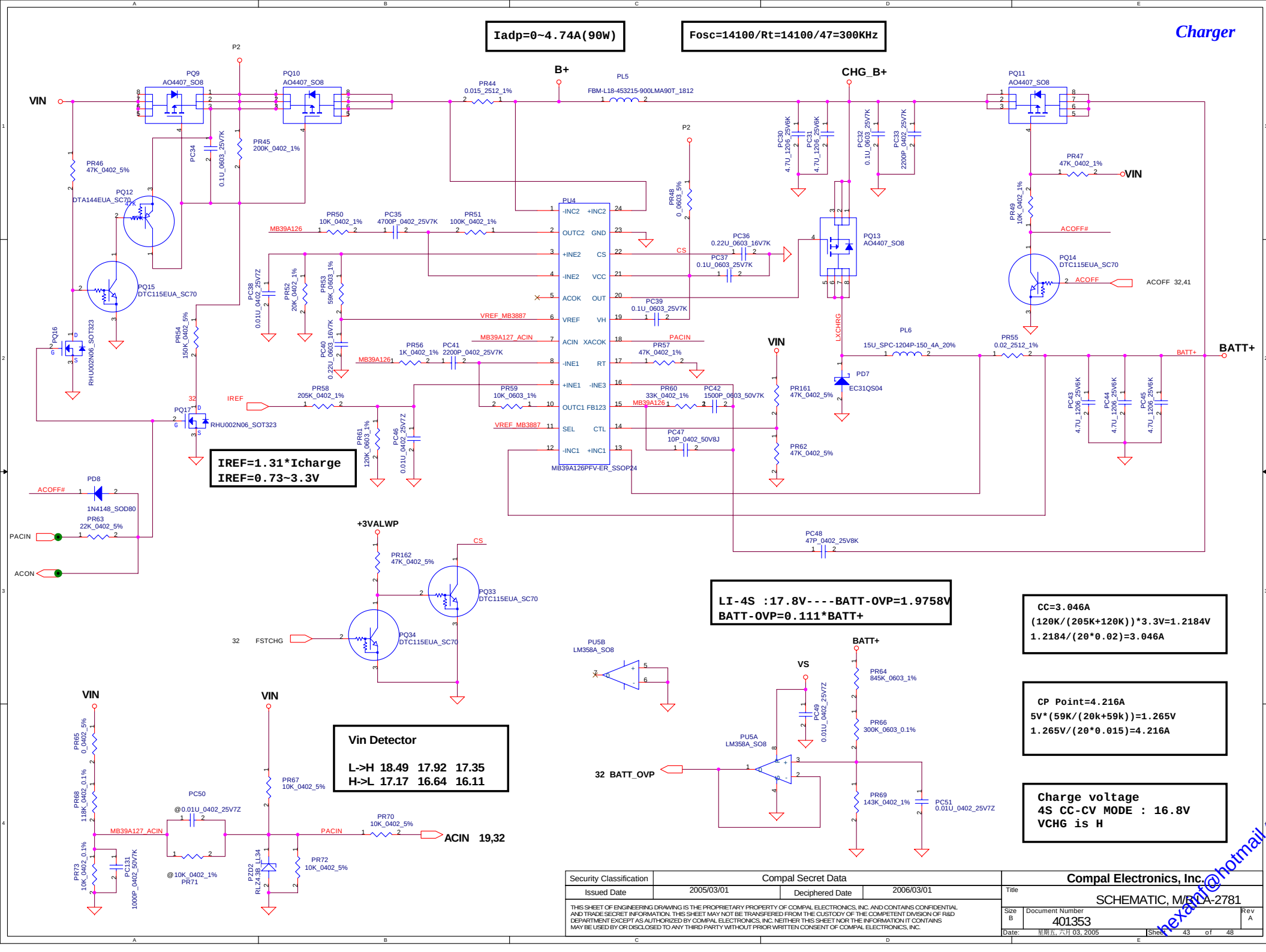
Charger

Iadp=0~4.74A(90W)

Fosc=14100/Rt=14100/47=300KHz



IREF=1.31*Icharge
IREF=0.73~3.3V

LI-4S :17.8V----BATT-OVP=1.9758V
BATT-OVP=0.111*BATT+

CC=3.046A
(120K/(205K+120K))*3.3V=1.2184V
1.2184/(20*0.02)=3.046A

CP Point=4.216A
5V*(59K/(20k+59k))=1.265V
1.265V/(20*0.015)=4.216A

Charge voltage
4S CC-CV MODE : 16.8V
VCHG is H

Vin Detector

L->H	18.49	17.92	17.35
H->L	17.17	16.64	16.11

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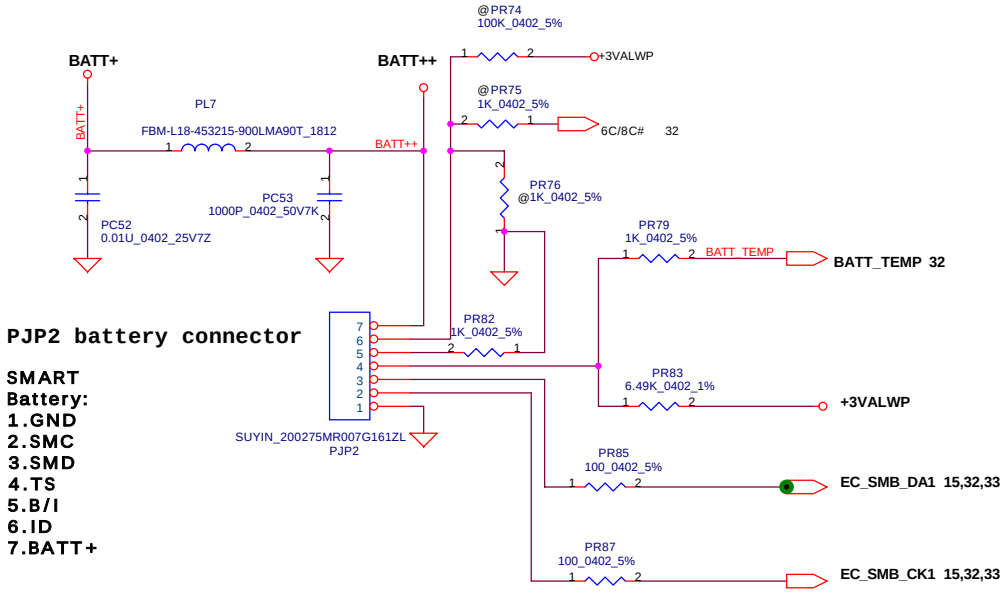
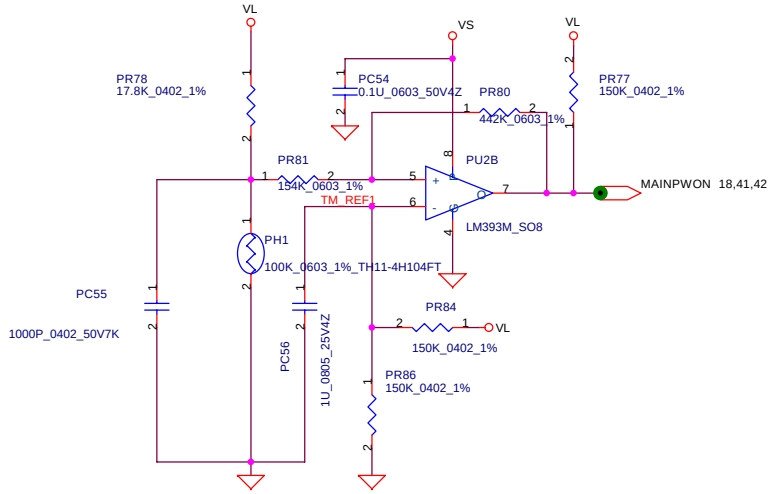
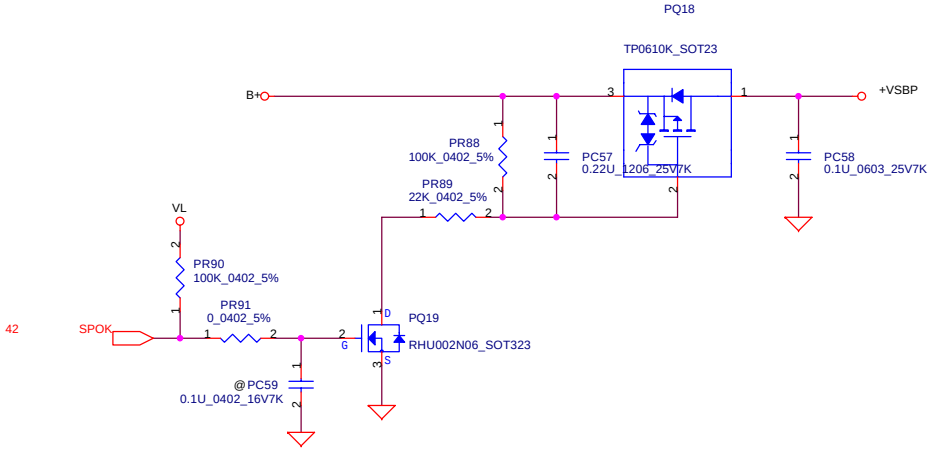


PJP2 battery connector

SMART Battery:
1.GND
2.SMC
3.SMD
4.TS
5.B/I
6.ID
7.BATT+

PH1 under CPU botten side :
CPU thermal protection at 80 degree C
Recovery at 44(45) degree C





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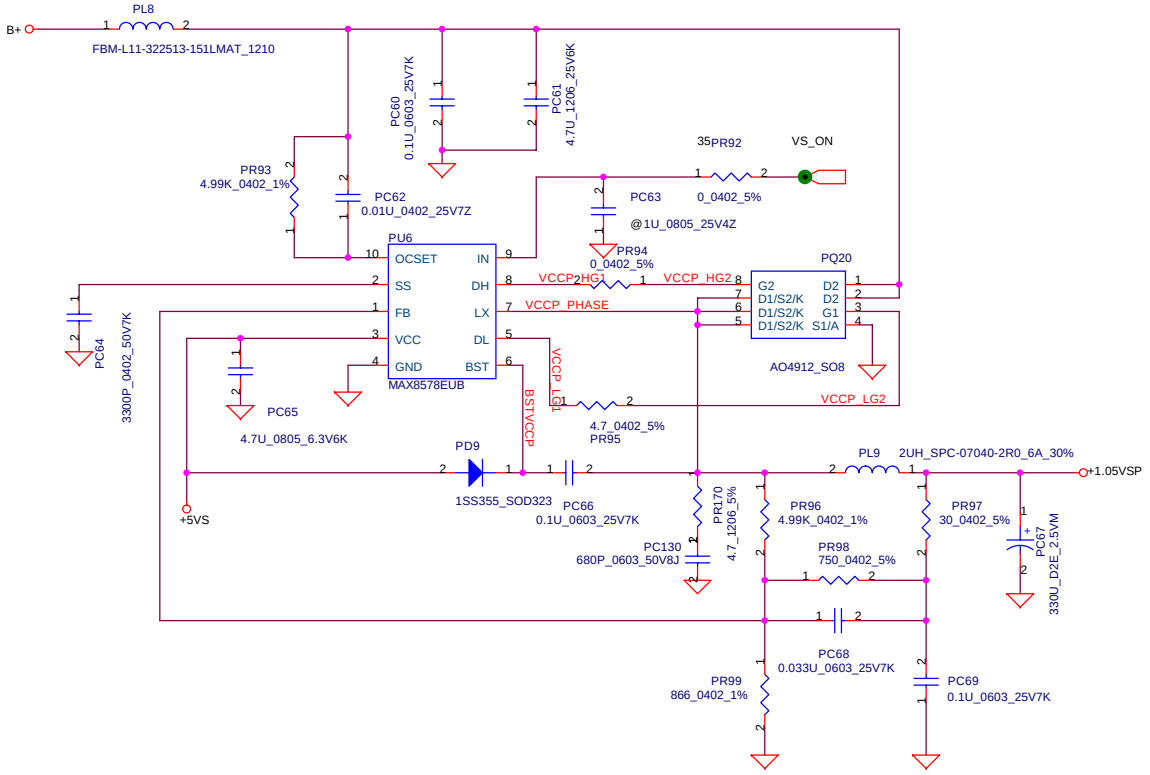

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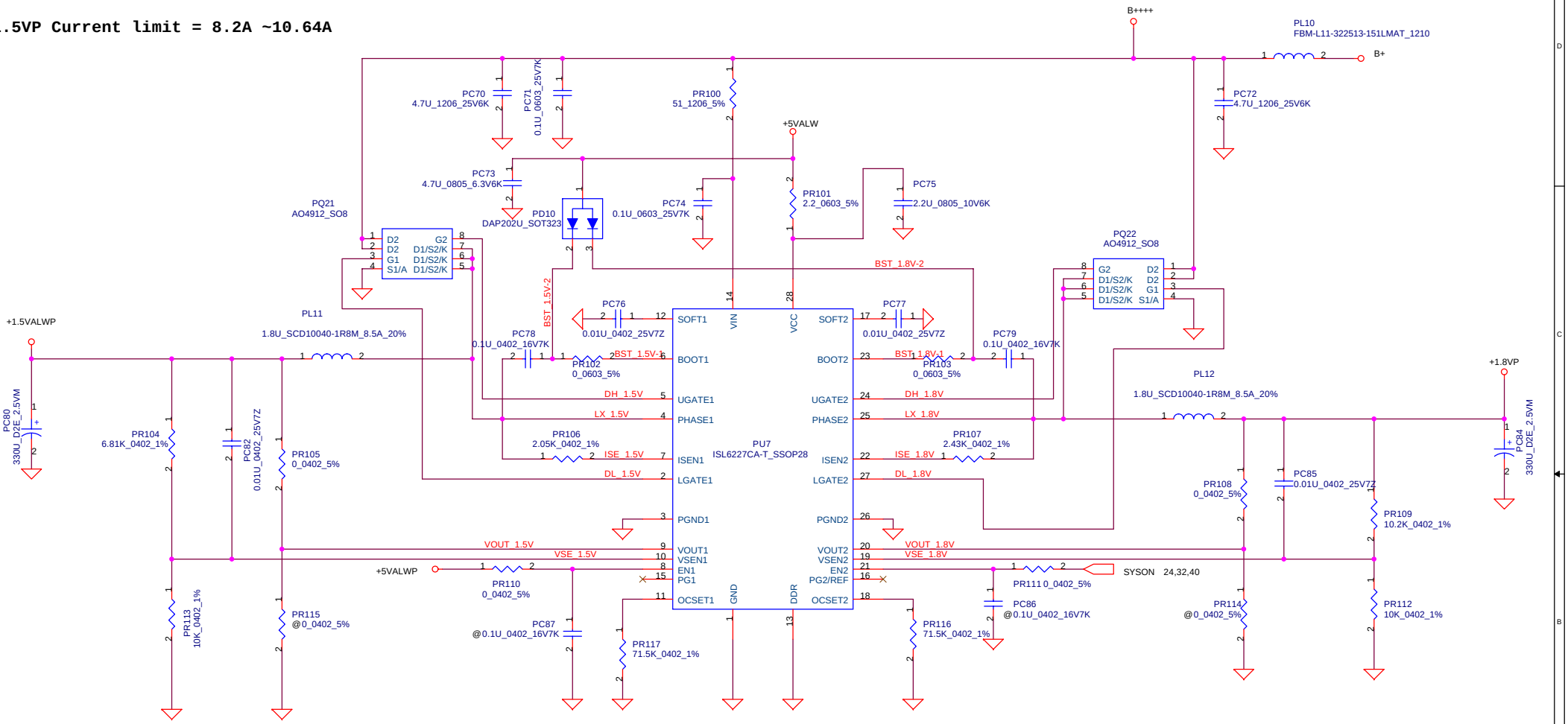
+1.8VP O.C.P. =8.1A ~ 10.36A

+1.5VP Current limit = 8.2A ~10.64A



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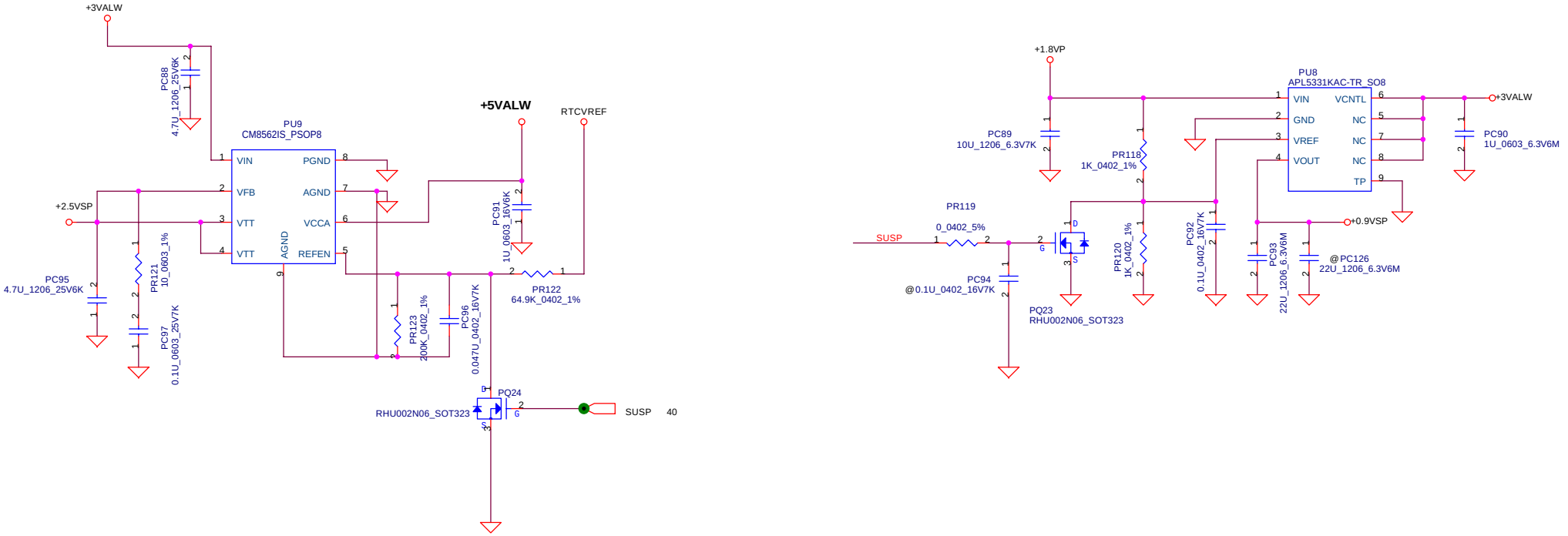

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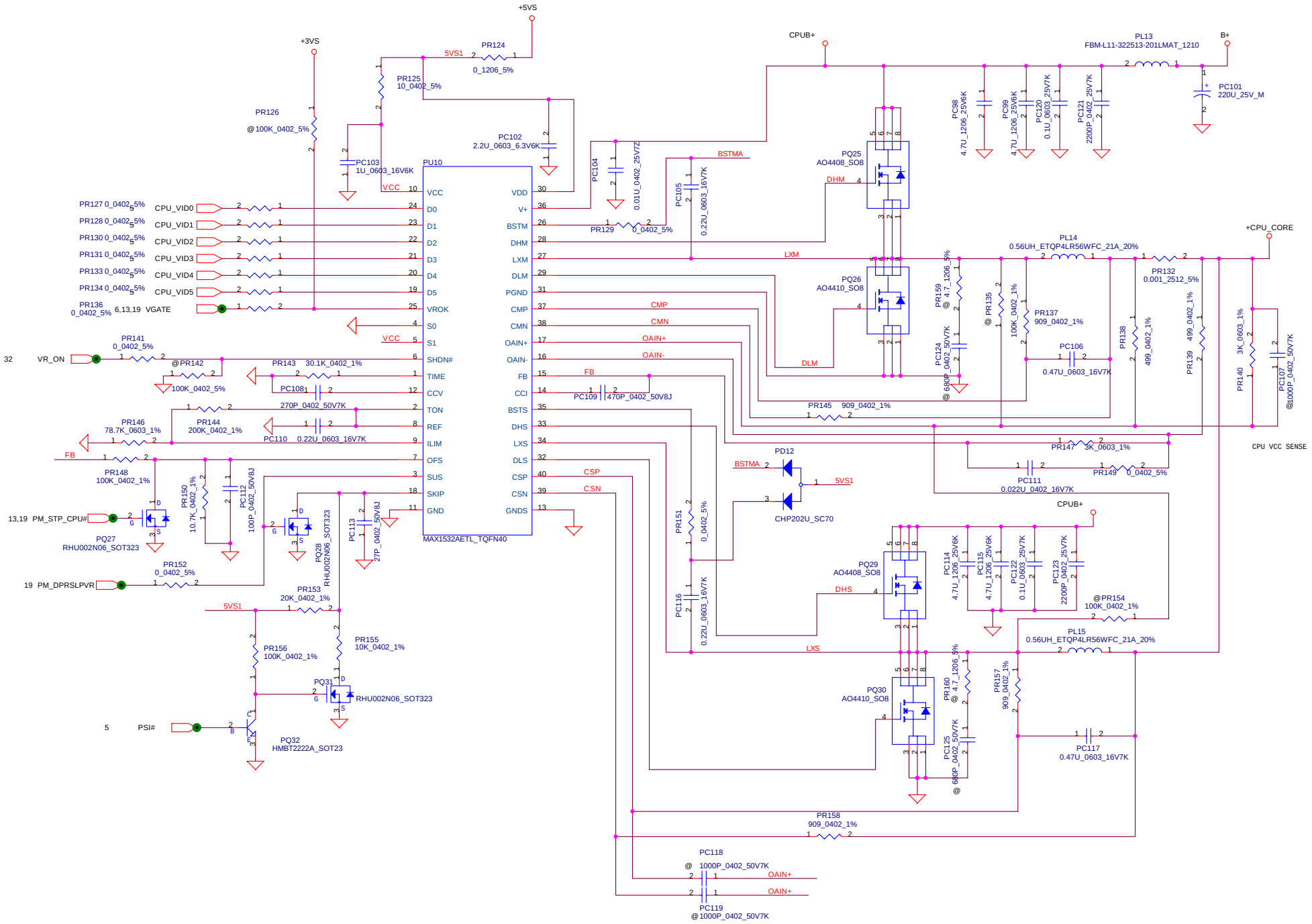

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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	B.Ver#	Phase
1	For HDQ70, change RTC change current.	Because the charge cuurent needs to meet battery spec.	0.1	41	Change PR16 and PR17 from SD028300000 to SD028560000.	0.1	DVT
2	For HDQ70, change MAX1999 to MAX8734A	Because MAX1999 has triggered UVP when AC Adapter plug in or plug out.	0.1	42	Change PU3 from SA019990000(S IC MAX1999EEI QSOP28 PWM) to SA00000G100(MAX8734AEEI+ QSOP 28P)	0.1	DVT
3	For HDQ70, fix Vin detector accuracy.	For HDQ70, fix Vin detector accuracy.	0.1	43	Change PR65 from SD034150200(S RES 1/16W 15K 0402 1%) to SD034000000(S RES 1/16W 0 0402 1%).	0.1	DVT
4	For HDQ70, fix Vin detector accuracy.	For HDQ70, fix Vin detector accuracy.	0.1	43	Change PR68 from SD034100300(S RES 1/16W 100K 0402 1%) to SD000008A00(S RES 1/16W 118K 0402 0.1%).	0.1	DVT
5	For HDQ70, fix Vin detector accuracy.	For HDQ70, fix Vin detector accuracy.	0.1	43	Change PR73 from SD034100200(S RES 1/16W 10K 0402 1%) to SD0000008B00(S RES 1/16W 10K 0402 0.1%).	0.1	DVT
6	For HDQ70, fix the battery temp curve.	Because we need to improve the curve of temp detector of battery more smoothly.	0.1	44	Change PR83 from SD034255200(S RES 1/16W 25.5K 0402 1%) to SD034649100(S RES 1/16W 6.49K 0402 1%).	0.1	DVT
7	For HDQ70, change 1.05VSP OCP point.	For HDQ70, change 1.05VSP OCP point.	0.1	45	Change PR93 from SD034412100(S RES 1/16W 4.12K 0402 1%) to SD034499100(S RES 1/16W 4.99K 0402 1%).	0.1	DVT
8	For HDQ70, fix the output voltage.	For HDQ70, fix the output voltage within spec.	0.1	45	Change PR96 from SD034715100(S RES 1/16W 7.15K 0402 1%) to SD034499100(S RES 1/16W 4.99K 0402 1%).	0.1	DVT
9	For HDQ70, fix the FB voltage.	For HDQ70, fix the FB voltage within spec.	0.1	45	Change PC68 from SE075682K00(S CER CAP 6800P 25V +-10% X7R 0402) to SE042333K00(S CER CAP .033U 25V K X7R 0603).	0.1	DVT
10	For HDQ70, add snuber on LX.	Add snuber on LX to improve high side noise.	0.1	45	Add PR170 SD011470BT9(S RES 1/10W 4.7 +-5% 1206).	0.1	DVT
11	For HDQ70, add snuber on LX.	Add snuber on LX to improve high side noise.	0.1	45	Add PC130 SE024681J00(S CER CAP 680P 50V J NPO 0603).	0.1	DVT
12	For HDQ70 1.5VALWP ripple voltage is too large.	Because we need to improve the ripple of 1.5VALWP.	0.1	46	Change PC80 from SGA20151330 to SGASGA19331D00.	0.1	DVT
13	For HDQ70, 1.8VP ripple voltage is too large.	Because we need to improve the ripple of 1.8VP.	0.1	46	Change PC84 from SGA20151330 to SGASGA19331D00.	0.1	DVT
14	For HDQ70, change 1.8VP OCP point.	For HDQ70, change 1.8VP OCP point.	0.1	46	Change PR107 from SD034174100(S RES 1/16W 1.74K 0402 1%) to SD034243100(S RES 1/16W 2.43K 0402 1%)	0.1	DVT
15	For HDQ70, change 1.8VP OCP point.	For HDQ70, change 1.8VP OCP point.	0.1	46	Change PR116 from SD034806200(S RES 1/16W 80.6K 0402 1%) to SD034715200(S RES 1/16W 71.5K 0402 1%).	0.1	DVT
16	For HDQ70, fix the 2.5VSP's power sequence.	Because we need to fix the power sequence of 2.5VSP.	0.1	47	Change PC96 from SE075222K00(S CER CAP 2200P 25V +-10% X7R 0402) to SE076473K00(S CER CAP 0.047U 16V K X7R 0402).	0.1	DVT

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Version change list (P.I.R. List)

HW section

Item	Reason for change	PG#	Modify List	Date	
1	AC_IN Signal	P.32	Remove R189, D11		DVT(Rev01)
2	LAN LED on 8110SBL	P.26	Unpop R449 on both 8100CL and 8110SBL		DVT(Rev01)
3	Modify +1.8VS and +1.5VS power sequence	P.40	Change R531,R551 value from 100K to 180K		DVT(Rev01)
4	5 Way BTN problem	P.33,34	Add 5WAY_BTN signal and R184		DVT(Rev01)
5	Remove New Card circuit	P.24	Remove New Card Circiut		DVT(Rev01)
6	New Card Clock Request	P.13	Connect PCIE_CLKREQ1# to Clock Gen pin.32		DVT(Rev01)
7	Change IEEE1394 Connector	P.25	Change IEEE1394 Connector Type		DVT(Rev01)
8	Codec VREF capacitor	P.36	Change C497 value from 0.1uf to 10uf		DVT(Rev01)
9	+SD_VCC and +XD_VCC Power Switch	P.23	Add R572, R573 for SD, XD Power Switch		DVT(Rev01)
10	Un-used Codec Clock	P.13	unpoped R89		DVT(Rev01)
11	Un-used ODD Connector	P.21	Remove the JP47 and C362,C366,C675,C678,C681		DVT(Rev01)
12	Add 10uF capacitor on GMCH	P.9	Add C703 on +3VS_DAC		DVT(Rev01)
13	Changed for Speaker and Subwoofer	P.37,38	Change Main Amplifier Gain form 10dB to 8dB, and Modify Woofer BPF value		DVT(Rev01)
14	Change CRT and TV-out Pi Filter Value	P.14	Change CRT and TV-out Pi Filter Value to Following Chipset Recommand		DVT(Rev01)
15	Change DVI SMBUS Pull-up Value	P.16	Change R346,R348 from 30K to 6.8K		DVT(Rev01)

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